Signal & Power Integrity Analysis Services for Test boards

Caliber Interconnect Solutions (Pvt) Ltd
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Mission & Vision

Mission

“Provide dependable solutions to the satisfaction of the customers through intensive R&D and proven quality control procedures using disciplined workforce.”

Vision

“Developing and applying technological solutions to the benefits of the society that will not affect the safety and living standards of our future generations.”

Quality Policy

“CALIBER INTERCONNECT SOLUTIONS PRIVATE LIMITED is committed to meet and exceed customers expectations through timely delivery of cost effective quality designs through ever improving process and team work.”
CONTENT

• About Caliber
• Business
• Signal Integrity Analysis
• ATE board types and analysis performed
• SI Analysis for SERDES & Loopback Channels
• DDR4 Analysis for Evaluation Board
• DC Analysis for Power nets
• Power Impedance and Caps Optimization Analysis
ABOUT CALIBER

• Caliber is a fast growing technology services company.
• Expertise is High speed PCB, Test boards, IC package design.
• Highly proficient in Signal Integrity, Power Integrity, EMI/EMC analysis.
• Specializes in Embedded design services, ATE hardware & Thermal analysis.
• 200+ highly skilled engineers.
• High quality & timely deliverable with attractive cost.
• Highest customer satisfaction.
OUR BUSINESS

- SEMICONDUCTOR
- CONSUMER ELECTRONICS
- AEROSPACE & AUTOMOTIVE
- COMMUNICATION & MILITARY

- IC PACKAGE
- HIGH SPEED BOARDS
- TEST BOARDS
- SIGNAL INTEGRITY
- EMBEDDED DESIGN
- THERMAL ANALYSIS
We Work closely with

- ATE Test system vendors
- Test interface board vendors and design houses
- Test houses and socket manufacturers
- Probe card assembly and design houses
- IC packaging design, manufacturing and assembly houses
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SOLUTIONS

- Lumped circuit analysis -> Transmission line analysis
- Full-wave Electromagnetic modeling of all Interconnects (via, connector, microstrip, stripline etc.)
- S-parameter modeling
- Crosstalk & Channel loss analysis
- Power-Distribution-Network (PDN) analysis
  (DC analysis, AC analysis, decoupling estimation)
- Jitter analysis (switching noise, Crosstalk, ISI)
- Eye-diagram plotting
- EMI/EMC analysis

Use state-of-the-art modern simulation tools
SIGNAL INTEGRITY CO-DESIGN

Minimize-cost & Maximize Performance
SERVICES

Signal Integrity
• Pre layout & Post layout
• Serial & parallel interface (DDR 2/3/4, gigabit-SERDES)
• Co-design (IC/package/board)
• IBIS/IBIS-AMI based system SI
• Crosstalk, channel loss, s-parameter, eye-diagram, timing analysis

Power Integrity
• DC Analysis (IR drop, voltage/current distribution, density plots)
  ● AC Analysis (PDN impedance analysis, target impedance optimization, Transient noise estimation)
• Decoupling cap analysis & optimization

EMI/EMC
• EMI Radiation
• EMI Susceptibility
• Compliances to various EMI standards during design phase

Simulation Tools
• Cadence Sigrity PowerDC, PowerSI, Optimize PI
• Ansys HFSS, Siwave, Designer
• Agilent ADS

Caliber Interconnect Solutions Pvt Ltd
ATE BOARD TYPES

Our ATE design services are exclusive for test interface board vendors, designers and ATE test system manufacturers.

- Load boards, Handler Interface Boards and Spider cards
- Probe cards & PIB (Probe Interface Boards)
- Bench Boards & Evaluation Boards
- Daughter cards (customized SUB boards for Load / Probe boards)
- Flexible PCBs (SUB boards in Probe cards to carry high speed signals, directly from Tester to Die)
Techs & Specs explored

Interfaces explored over a ATE environment

- DDR (2, 3 & 4)
- USB
- PCIe
- SATA
- HDMI
- LVDS
- SerDes
Techs & Specs explored

AGILENT 93K - LOAD BOARD

USB3 Loopback with ground shielding and stitching vias
Techs & Specs explored

Ultraflex – LOAD BOARD

SERDES Channel

DDR2 Signals
Techs & Specs explored
Techs & Specs explored

Design with RF signals
Techs & Specs explored

Design recommendations based on SI-PI analysis

Ground fencing via are added for RF signals in order to reduce radiation

Tapered trace for neck down in order to reduce the reflection

Bigger Trace (24 mils) in order to reduce skin effect loss and matching the PAD size
○ The impedance analysis is done using PolarSI.
○ Impedance is verified for the given stack up and trace parameters.

Microstrip Neck-down condition.

Microstripline condition.
Via modeling and simulation is done using Ansys HFSS tool.

HFSS is to model 3D structure and to find the best via structure for high speed signals to match the target impedance.
Studying via stub effect for high frequency signals, based on which the back drilling needs will be defined.

Via with stub - Both the RL and IL is affected when frequency is increased above 1 GHz

Via without stub - Both the RL and IL is very much improved.
Via impedance control using coupled vias are studied for high speed signals and implemented if needed.
Insertion loss for 5Gbps SERDES channel

RED : Nelco 4000 -13 Dielectric material
BLUE : FR4 Dielectric material
Return loss for 5Gbps SERDES channel

RED : Nelco 4000-13 Dielectric material  BLUE : FR4 Dielectric material
TDR for 5Gbps SERDES channel

RED : Nelco 4000-13 Dielectric material  BLUE : FR4 Dielectric material
USB3 Loopback simulation
USB3 Loopback Channel – Insertion & Return Loss

Insertion Loss

Return Loss

Company confidential

Caliber Interconnect Solutions Pvt Ltd
SATA Loopback Channel – Insertion & Return Loss

Insertion Loss

Return Loss

Company confidential
DDR4 Timing Analysis in Evaluation Board

Processor

800 MHz
- IO Buffer

800 MHz
- IO Buffer

800 MHz
- IO Buffer

PKG model

PCB MODEL

DDR4 ibis

- DRAM

- DRAM

- DRAM

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DDR4 Timing Analysis

Evaluation board

Data signal quality
The minimum voltage swing is 186 mV
The maximum RX eye mask is 136 mV (eye mask height).
The required timing window for valid data window is 0.2UI which is 125 ps for 1600 Mbps data rate (eye mask width).
DATA Write cycle - 48DSE/34 ODT
- **IR drop analysis** – to find voltage drop for plane and pins and to find the hot spot areas
- **Power/GND Impedance profile analysis** – The target impedance is useful for sizing the amount of capacitance necessary at each level of assembly to store sufficient charge and energy for the load.
- **De-coupling Capacitors Estimation and Optimization** – It is necessary to analyze and optimize the exact number and values of capacitors needed in order to achieve the desired PDN
- **Power Plane RLC** – Proper control in the plane RLC value gives good power impedance with less IR drop.
PI- IR DROP SIMULATION

IR DROP Results before layout Modification

IR DROP Results after layout Modification

Note:
----- IRdrop on net is calculated on Power net only.
----- If a net has current flow from different sources, IRdrop is displayed with the largest IRdrop.
PI-IR DROP SIMULATION

Voltage distribution in Power Layer

Voltage distribution in GND Layer
Power Plane Impedance Analysis

Graph in Red color is the Impedance profile for original layout before Decap optimization. Blue color line is Target impedance.
Power Plane RLC – Inductance curve

Inductance (µH)

Frequency (MHz)
EMI/EMC Checking according to **CISPR** Class A Standard

**GENERAL INFORMATION**

- Board: BOARD_2.byp
- Total number of nets: 775
- Total number of components: 75
- Board temperature: 20.0 degrees C
- Default IC model (used for quick analysis if IC model is missing)
- IC driver rise/fall time: 2.000 ns
- IC driver switching voltage range: 3.00 V
- IC driver output impedance: 1.0 ohms
- IC input capacitance: 7.0 pF

**NET INFORMATION**

- Net = CH23
  - EMC SIMULATION RESULTS
  - Net's EMC is within selected limits

- Net = CH42
  - EMC SIMULATION RESULTS
  - Net's EMC is within selected limits

- Net = CH39
  - EMC SIMULATION RESULTS
  - Net's EMC is within selected limits

- Net = CH124
  - EMC SIMULATION RESULTS
  - Net's EMC is within selected limits

- Net = CH141
  - EMC SIMULATION RESULTS
  - Net's EMC is within selected limits

**EMC STANDARD CHECKING REPORT BASED ON CISPR**
**Global Presence**

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