IMPORTANCE OF POWER PLANE ORIENTATION

Presented @
CDNLive 2016
Cadence User Conference 2016
Bengaluru.
August 9

Authors:
Ashish Bhandari
Gowrisankar Arumugasamy
Sabari Siva Sankaran N
Shanmugapriya Devadasan

Caliber Interconnect Solutions Pvt. Ltd

- Caliber is a fast growing technology services company.
- Expertise in High speed PCB, IC package design.
- Highly proficient in Signal Integrity, Power Integrity, EMI/EMC analysis.
- Specializes in Embedded design services, ATE hardware & Thermal analysis.
- 200+ highly skilled engineers.
- High quality & timely deliverable with attractive cost.
- Highest customer satisfaction.

Services

Signal Integrity

- Pre layout & Postlayout
- Serial & parallel interface (DDR 2/3/4, gigabit-SERDES)
- Co-design (IC/package/board)
- IBIS/IBIS-AMI based system SI
- Crosstalk, channel loss, s-parameter, eye-diagram, timinganalysis

Power Integrity

- DC Analysis (IR drop, voltage/current distribution, density plots)
- AC Analysis (PDN impedance analysis, target impedance optimization, Transient noise estimation)
- Decoupling cap analysis & optimization

EMI/EMC

- EMI Radiation
- EMI Susceptibility
- Compliances to various EMI standards during designphase

Simulation Tools

- Cadence Sigrity PowerDC, PowerSI, Optimize PI
- Other EDAtools

Importance of PI Simulation

With the emergence of latest technologies,

- The power consumption of IC's has increased
- The voltage level of IC operation has decreased
- The target imposed on the PDN (Power Delivery Network) is getting tighter.

Added to this the ever decreasing real estate, adds to the worry of designers. The designers find it hard to pour extra copper for the power plane or to place the decaps and their via through a very dense layout. These difficulties require some innovative ideas to improve the performance of the PDN. It is at this juncture the Power Integrity guys have their say and help out the designers to achieve the target.

PI simulations help in optimizing the performance and doing detailed study on PCB without wasting a single penny on fab process.

Abstract

The two main parameters that decide the performance of PDN are,

DC IR Drop – cause the Voltage level to shift from ideal value

AC Power Impedance – cause the ripples in voltage during currenttransient.

▪Study the effect of copper area, power flow and orientation of the power planes on above two parameters.

▪This study will **break the myth** "to reduce the IR Drop the copper area has to be increased".

▪We have proved that, with same copper area but different orientations it is possible to improve the performance of the PDN almostby 100%.

▪No need to go for option that increase the cost

▪Just change the orientation and you have the PDN performance improved to meet the target.

Objective

- To study the importance of orientation of the power planes in deciding the performance of the PDN.

- To compare the performance of power net with same copper area, but with different orientation;
  - 1 Full power plane

    vs
  - 2 Half power planes.

- And to strongly establish the fact, "**it is the orientation of the power plane that is more important in deciding the performance of PDN rather than the copper area of power plane**".

- To perform this simulation we have used **Cadence Sigrity PowerDC** and **OptimizePI**.

Effect of Copper Area

- What is the relation between the resistance of below 2 square planes?

5 * 5 = 25mm square

1 * 1 = 1mm square

Effect of Copper Area

Different area, but same resistance value. As ALL SQUARE PLANE with same thickness have same resistance.

1 * 1 = 1mm square **0.428 mOhm**

5 * 5 = 25mm square **0.428 mOhm**

Effect of Power flow

- What is the relation between the resistance of below 2 planes?

5 * 5 25 mm square

2 * 12.5 25 mm square

Effect of Power flow

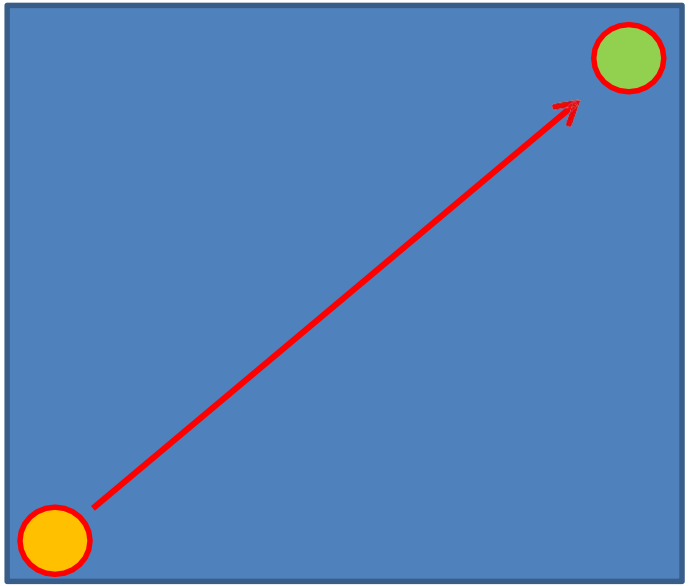
Same area, but different resistance value. Here the area of current flow defines the resistance.

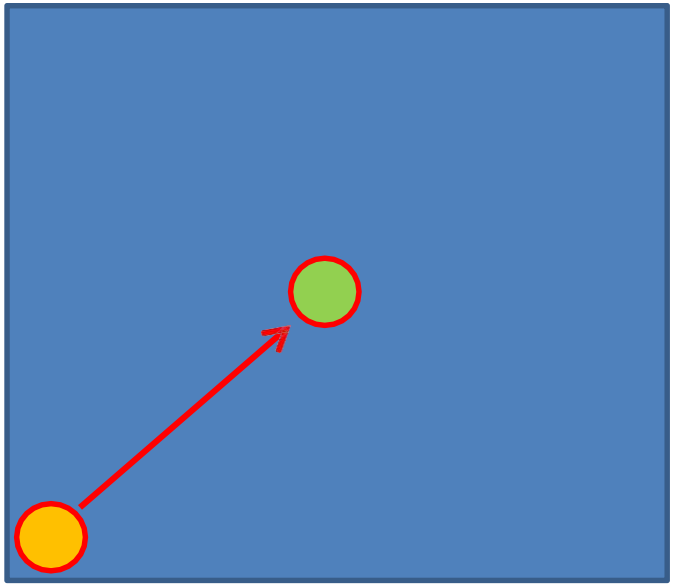
5 * 5 25 mm square **0.428 mOhm**

2 * 12.5 25 mm square **2.68 mOhm**

Effect of position of source and destination

- What is the current flow pattern between the below 2 cases?



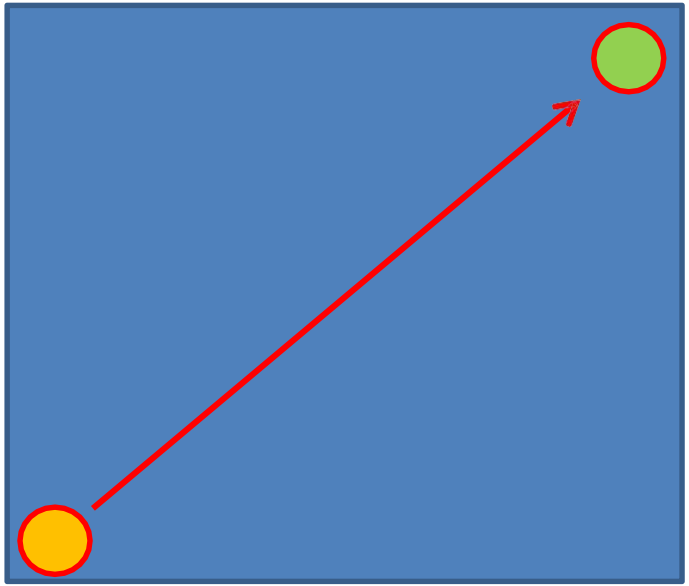


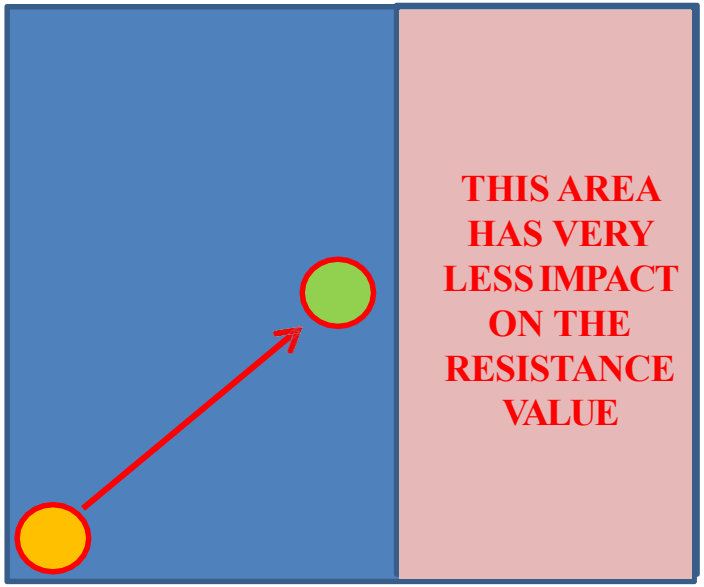
Source – Tester channel or Voltage Regulator

Destination – IC or DUT

Effect of position of source and destination

Only minimal current flows behind the destination





Source – Tester channel or Voltage Regulator

Destination – IC or DUT

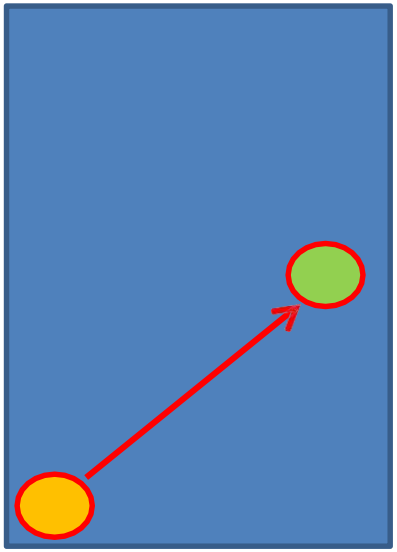
Summary

The copper area, power flow and power plane orientation affect the performance of the power planes at different level.

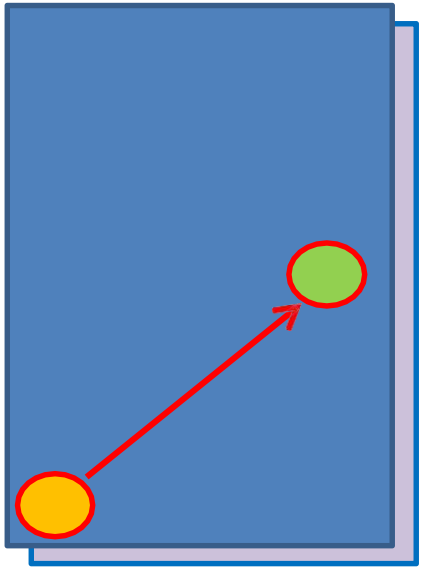
To study their effect, we considered 3 cases.

Various cases considered

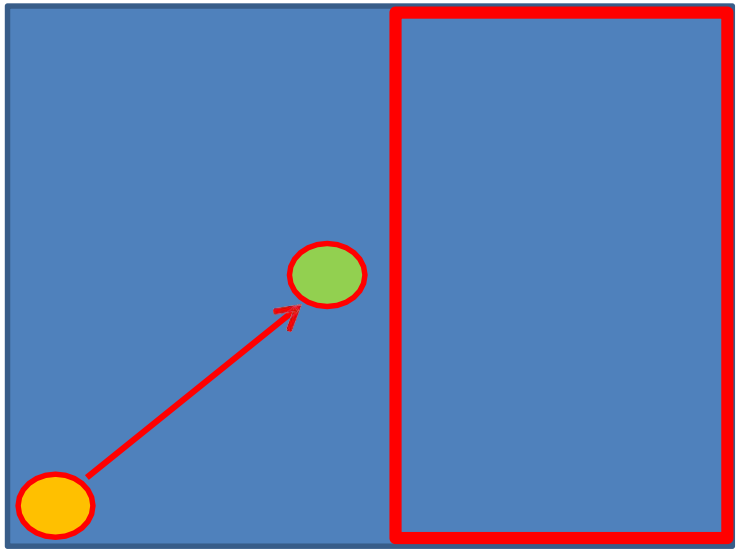
1 Half Plane



2 Half Plane



1 Full Plane



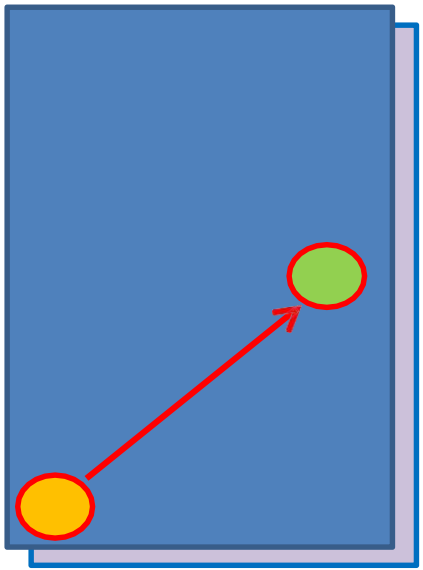
Source – Tester channel or Voltage Regulator

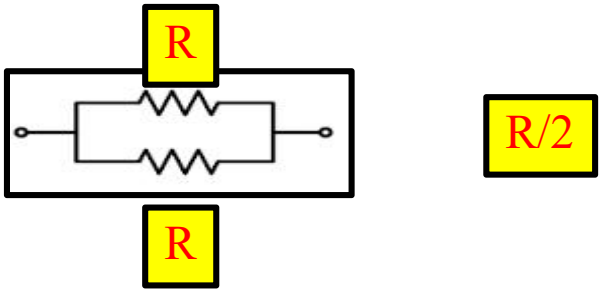
Destination – IC or DUT

Advantages of 2 Half Power Planes

A better performing Power Distribution Network should have,

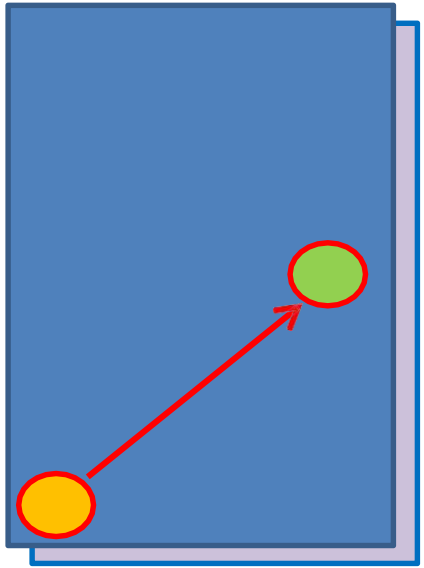
- Least Resistance
- Least Inductance
- Large Capacitance

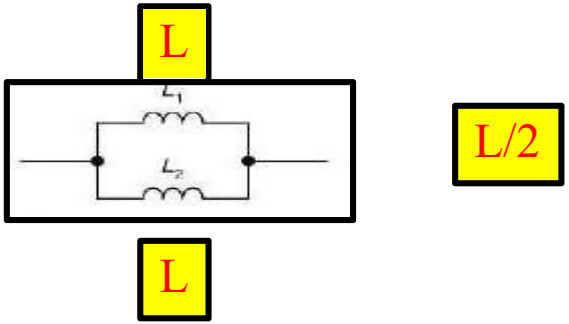




Advantages of 2 Half Power Planes

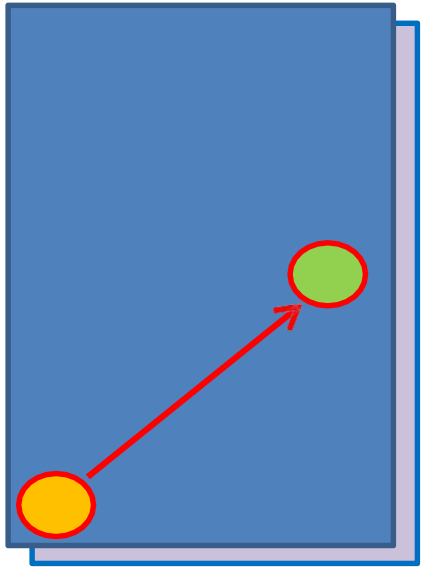
Parallel inductance have less inductance.

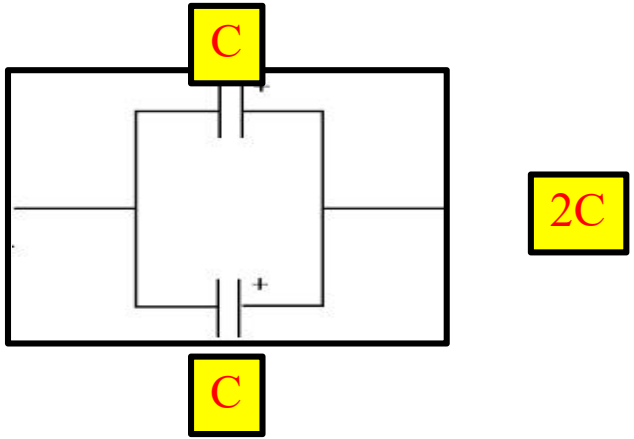




Advantages of 2 Half Power Planes

Parallel capacitance have more capacitance





Sigrity PowerDC & OptimizePI Simulations

Case Study: 1 Full plane

Electrical Simulation setup

PowerDC

Layout considered: For simplicity we have used, 2 DUT Load board

No. of layers: 44 layers (Thickness) 230 mil

Nets simulated: Power Net1 & Power Net2

VRM	VRM	VRM_J601_1_DGND	VRM_J801_2_DGND
	Component name	J601	J801
	Voltage (v)	0.9±0%	0.9±0%
	(+) net name	1	2
	(-) net name	DGND	DGND
	Sense line (+) node		
	Sense line (-) node		

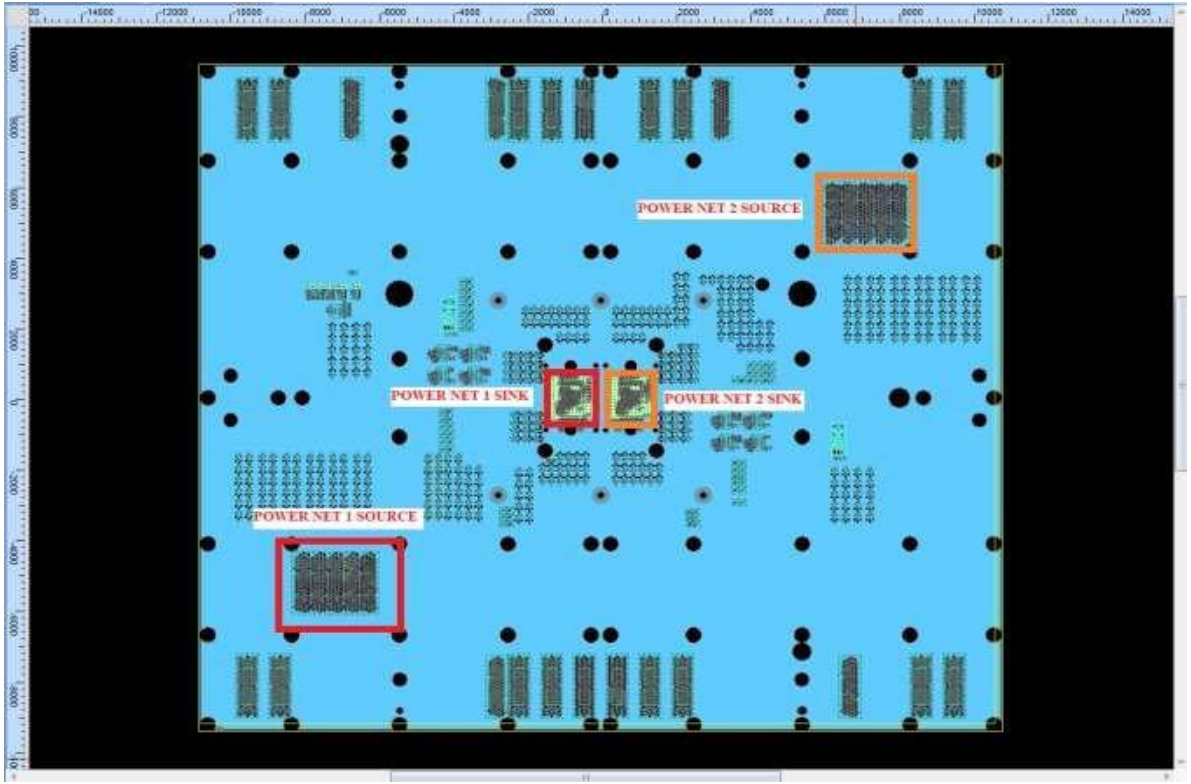
VRM Setup

Sink Setup

Sink	Sink	SINK_1BGA_1_DGND	SINK_2BGA_2_DGND
	Component name	1BGA	2BGA
	Voltage (v)	0.9-5%,0.9+5%	0.9-5%,0.9+5%
	(+) net name	1	2
	(-) net name	DGND	DGND
	DC current (A)	16	16
	Current model	Equal Current	Equal Current
	Fail/Pass model	Worst	Worst

1 FULL PLANE LAYOUT

PowerDC

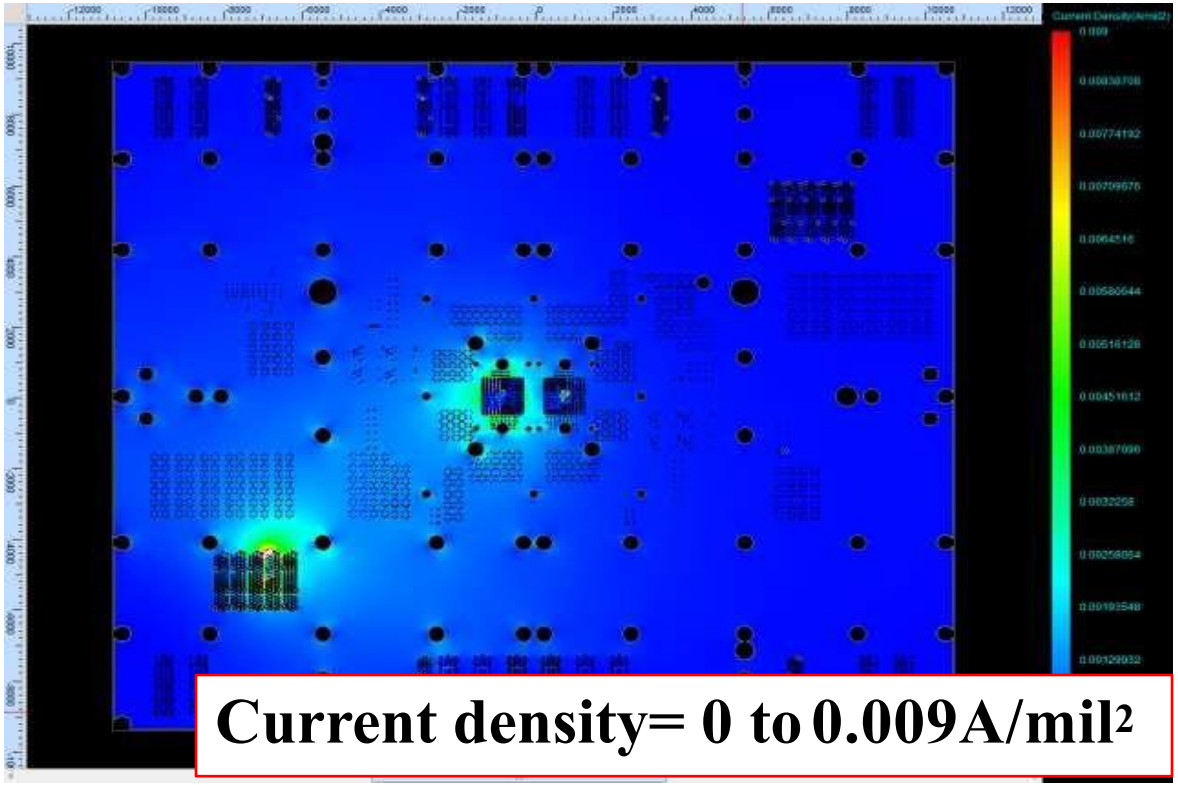


The power shapes are present in

Lyr15 – Power net1
Lyr16 - GND
Lyr17 – Power net2

Initially 1 Full plane for each of the net is considered

Current density plot of 1 Full plane of Power Net1



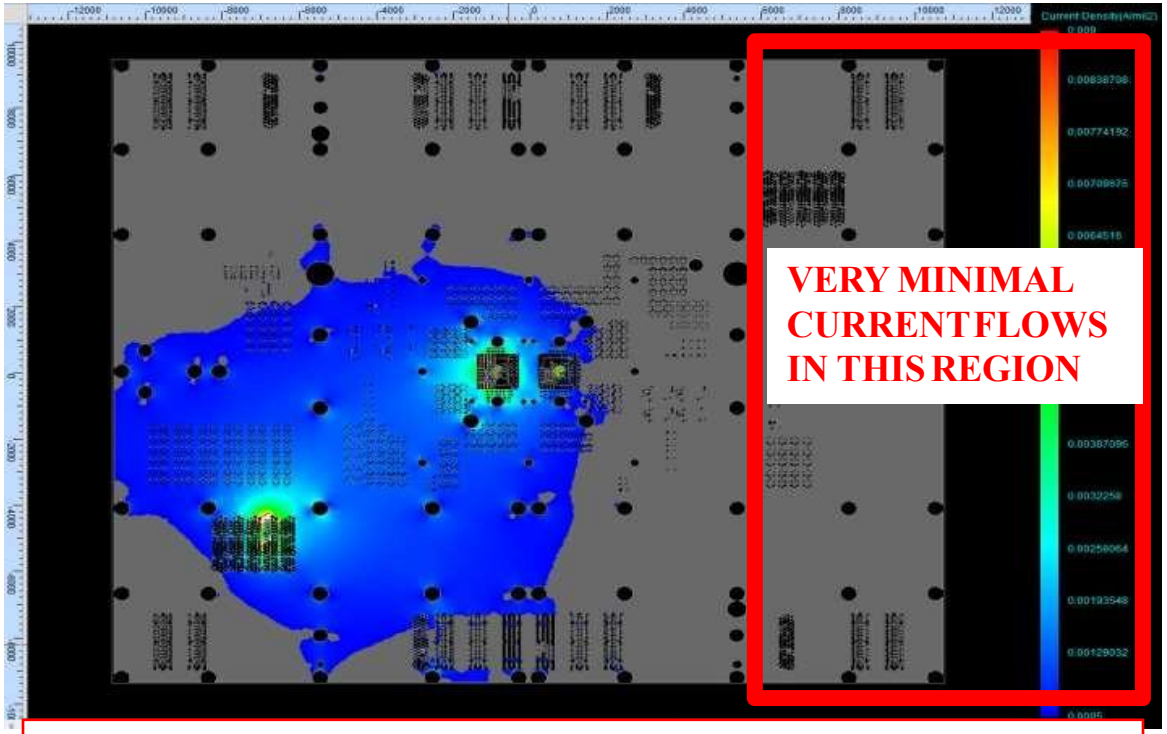
Current density= 0 to 0.009A/mil²

PowerDC

The image shows the current distribution between the source and destination.

It is observed that the current density is high near to the source & destination.

Current density plot of 1 Full plane of Power Net1



PowerDC

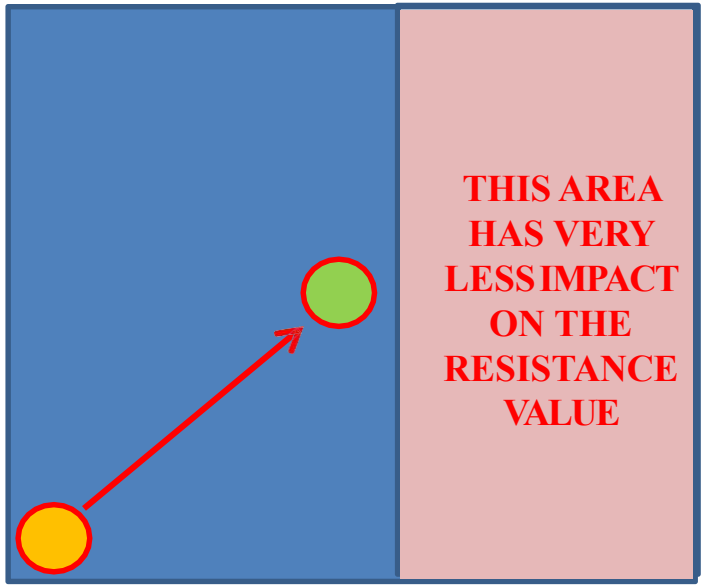
The same plot with different current density rating is shown here.

The region beyond the destination has minimal current through it

Current density= 0.0005 to 0.009A/mil²

Effect of position of source and destination

Hence it is proved that only minimal current flows behind the destination

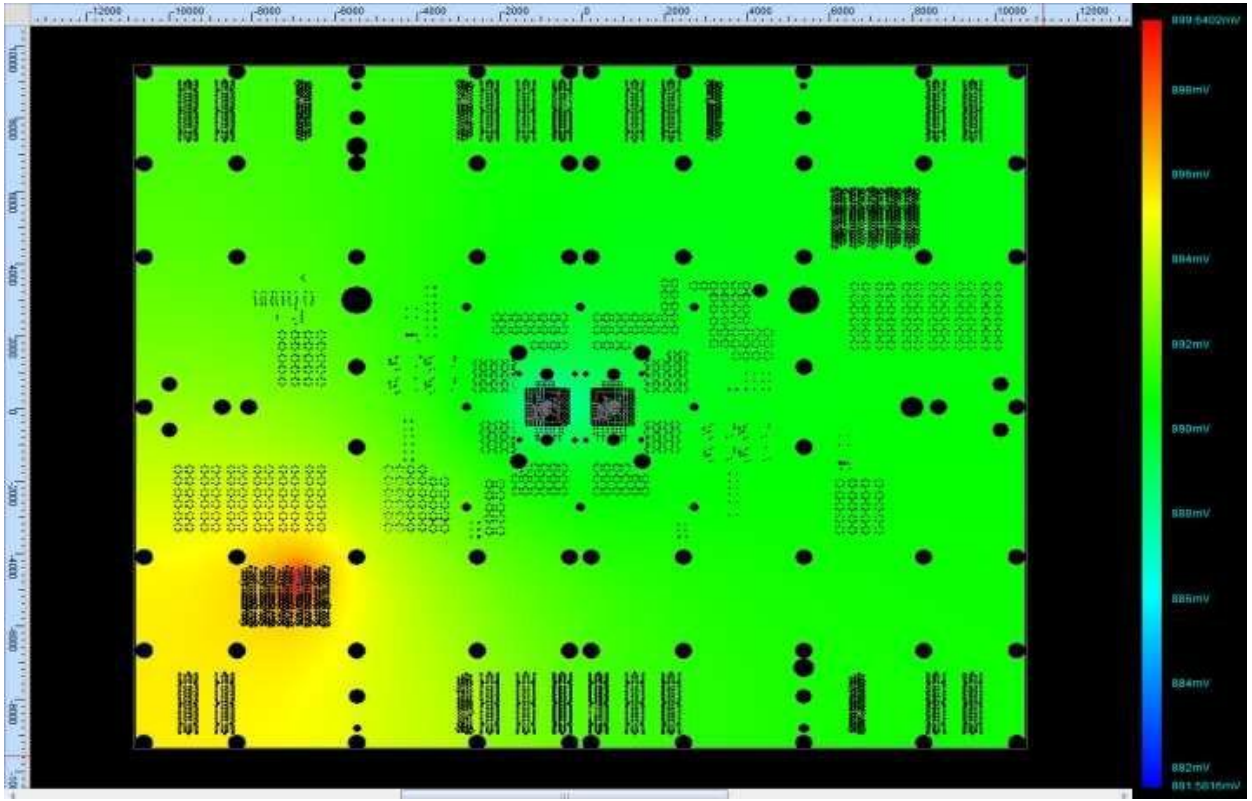


Source – Tester channel or Voltage Regulator

Destination – IC or DUT

Voltage plot of 1 Full plane of Power Net1

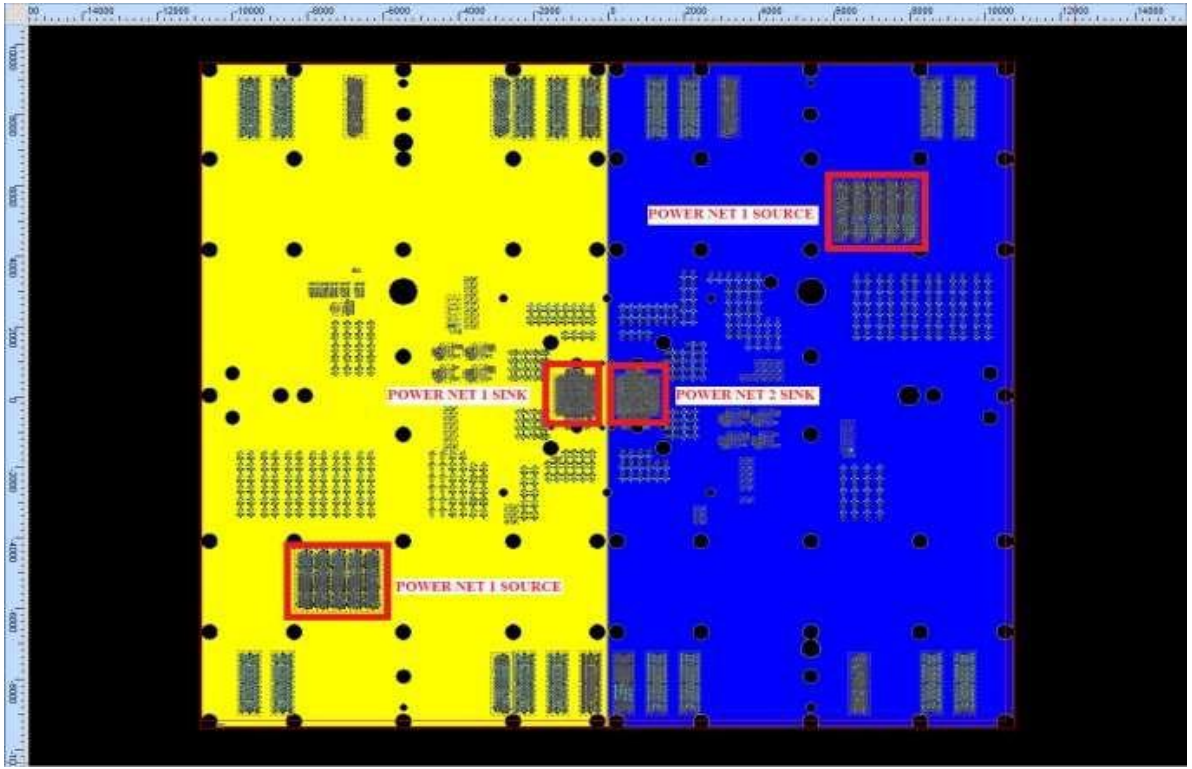
PowerDC



Case Study: 2 Half plane

2 HALF PLANE LAYOUT

PowerDC



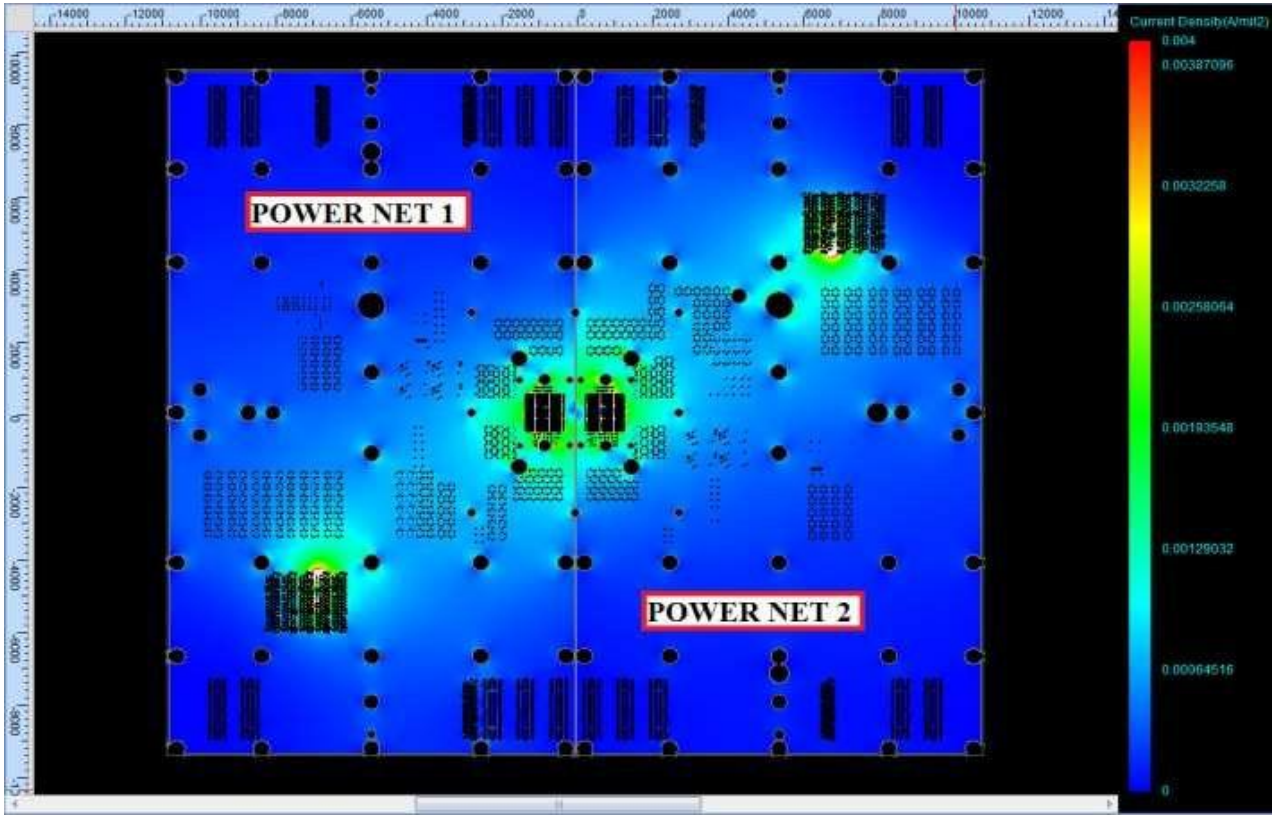
The power shapes are present in

Power net1- 2 Half planes on Lyr15 & Lyr17

Power net2- 2 Half planes on Lyr15 & Lyr17

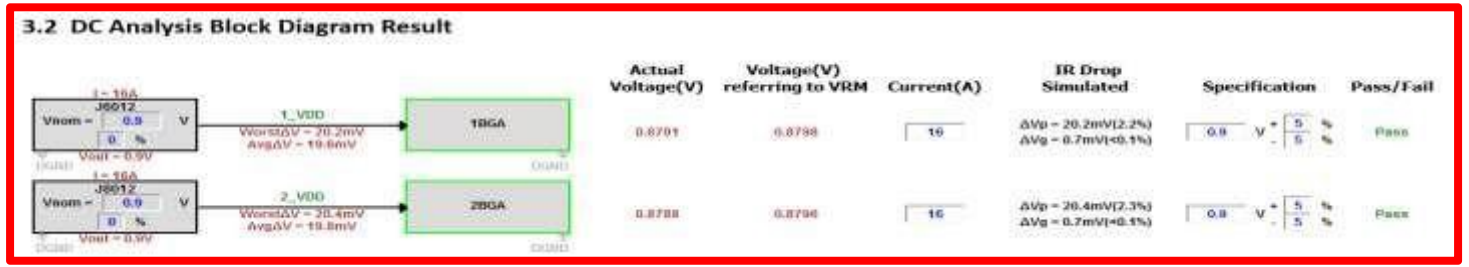
Current density plot of 2 half plane of Power Net1 & 2a

PowerDC

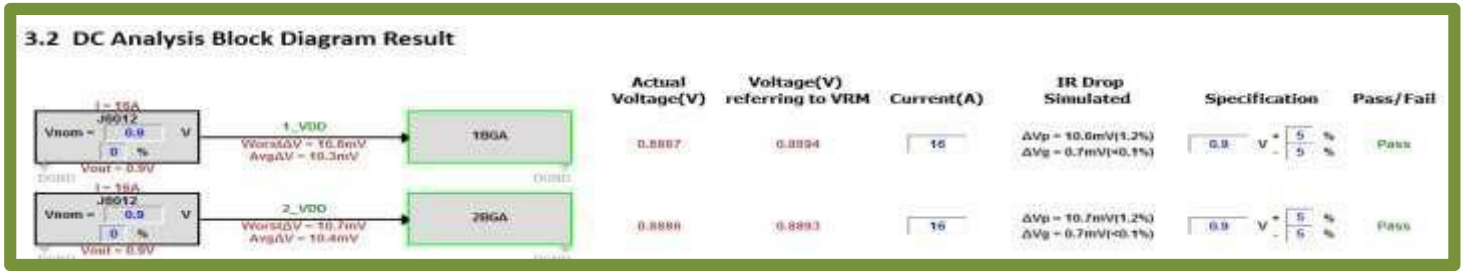


Sigrity PowerDC - Simulated results

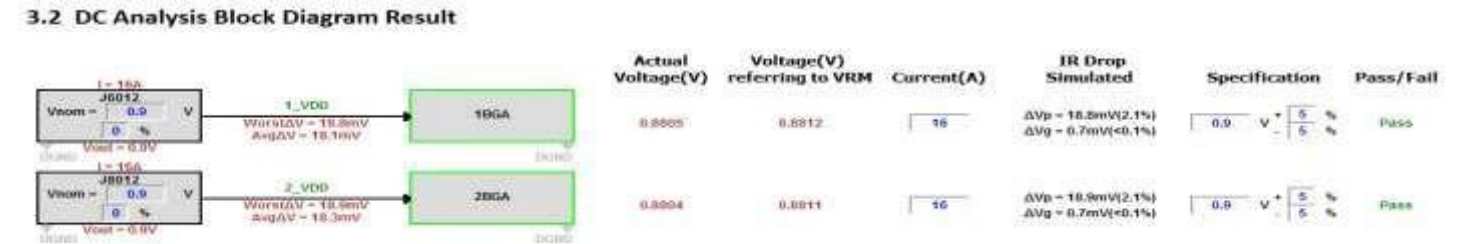
1 HALF PLANE



2 HALF PLANE



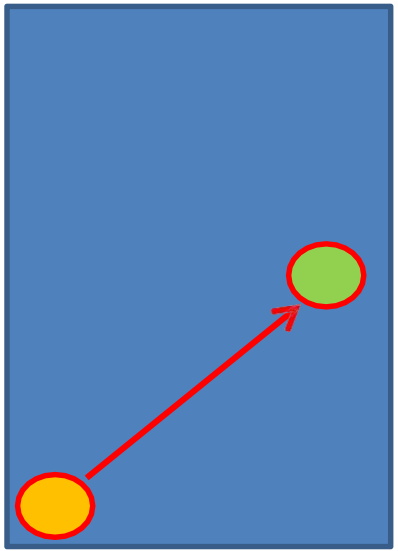
1 FULL PLANE



Sigrity PowerDC - Simulated results

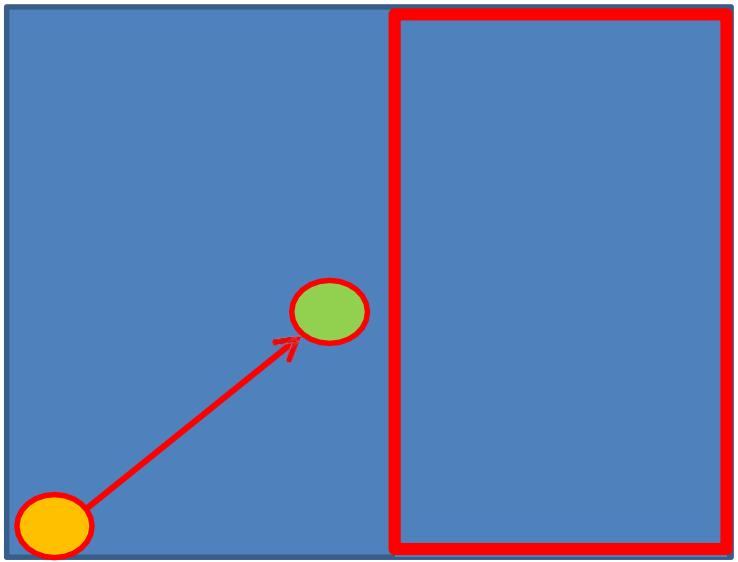
POWERNET 1	0.9V	16A

CASE	RESISTANCE (mOhm)	VOLTAGE DROP (mV)	VOLTAGE DROP PERCENTAGE (%)
1 HALFPLANE	1.25729	20.4	2.3
1 FULL PLANE	1.16288	18.9	2.1



DOUBLE THE COPPER AREA

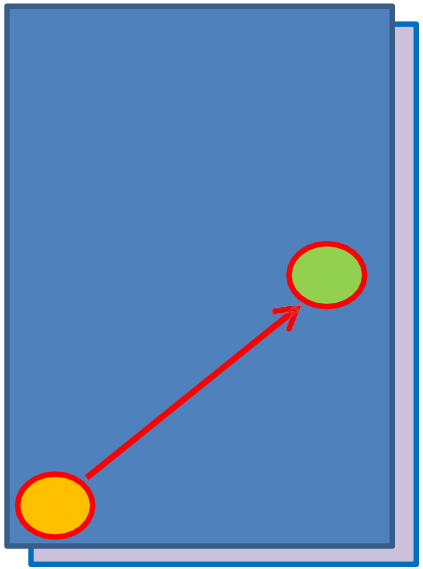
NOT MUCH IMPROVEMENT



Sigrity PowerDC - Simulated results

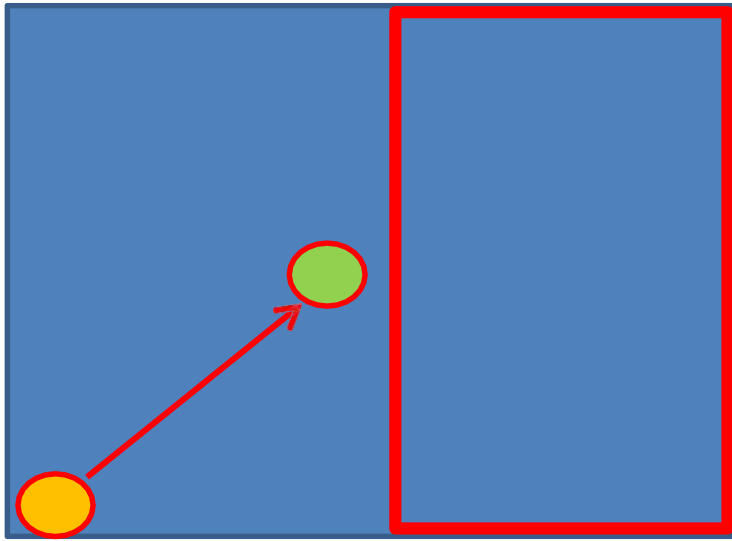
POWERNET 1	0.9V	16A

CASE	RESISTANCE (mOhm)	VOLTAGE DROP (mV)	VOLTAGE DROP PERCENTAGE (%)
2 HALFPLANE	0.681459	10.7	1.2
1 FULLPLANE	1.16288	18.9	2.1



SAME COPPER AREA DIFFERENT ORIENTATION

ALMOST 100% IMPROVEMENT



Sigrity PowerDC - Simulated results

POWERNET 1	0.9V	16A

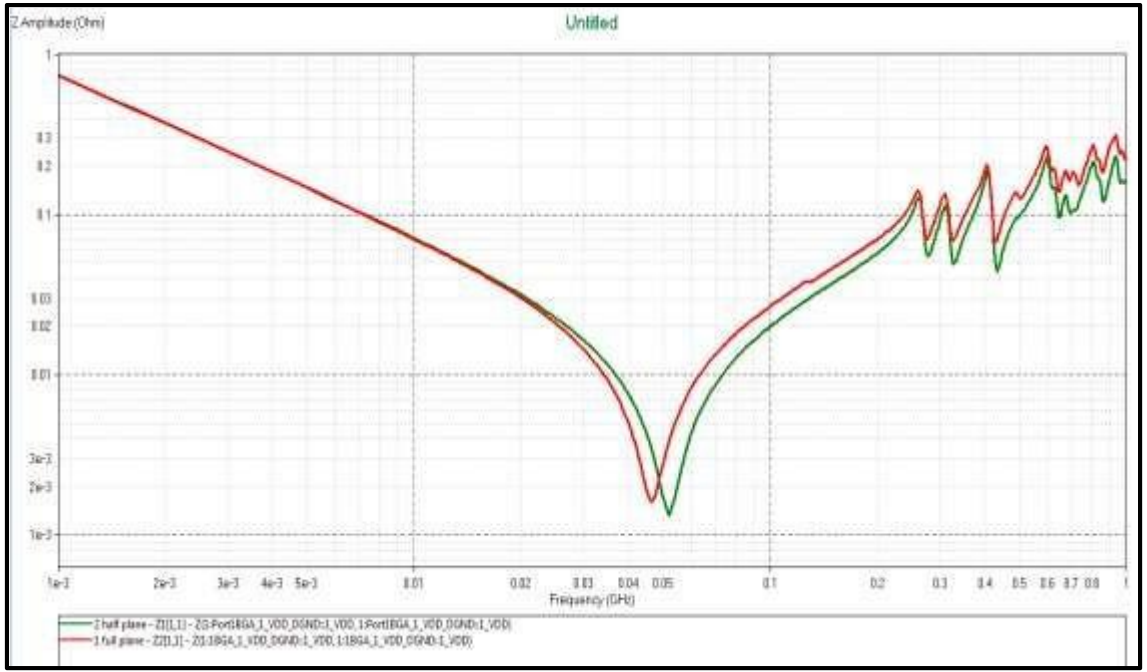
CASE	RESISTANCE (mOhm)	VOLTAGE DROP (mV)	VOLTAGE DROP PERCENTAGE (%)
1 HALFPLANE	1.25729	20.4	2.3
2 HALFPLANE	0.681459	10.7	1.2
1 FULLPLANE	1.16288	18.9	2.1

As in theory, the simulation result also confirm that with same copper area but with different orientation, we can achieve better performance.

This study strongly establish the fact, "**it is the orientation of the power plane that is more important in deciding the performance of PDN rather than the copper area of power plane**".

Power Impedance Z11- AC analysis

OptimizePI / PowerSI



•The graph shows the power impedance Z11 profile of the power planes without any VRM or Decaps.

•The cases of 1 full plane **(Red)** and 2 half planes are compared.

•The case of 2 half plane **(Green)** has a slightly lower impedance and higher anti-resonant frequency.

Summary of study

•With same copper area, but with different orientation of the power plane, the performance of the power planes can be improved.

•As of now, we have implemented this pattern in the layouts and have achieved better performance.

•As a next step we will explore this effect further in a complex way by combining the effects of the decaps and the placement of decaps and other factors.

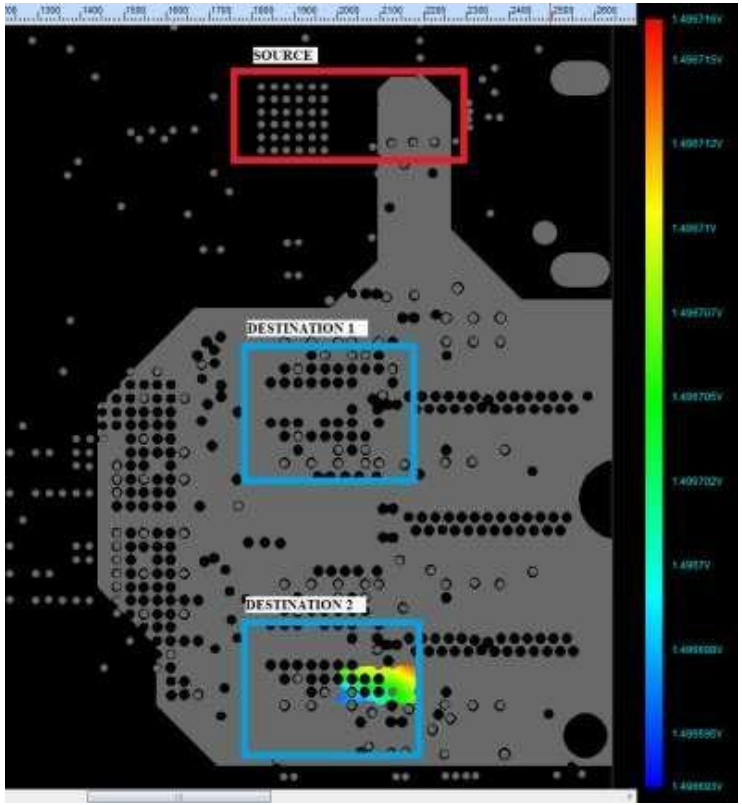
OTHER FEATURES TO OPTIMIZE IR DROP

Optimal Sense pin Location

- Sense nets are used to compensate the voltage drop in the power plane. The voltage is sensed near to the sink component, so that it can be feedback to the regulator and the voltage drop can be compensated.
- It is difficult to locate the best location to sense the voltage, in caseswhere more components are supplied by same power net.
- The tool help us to locate the exact spot to sense the voltage so that the feedback caters to the need of all the components.
- Optimal sense location can yield 10-30% margin improvement.

Voltage plot of optimal Sense pin Location

PowerDC



- Here we have considered a case of DDR interface with 2 DDR memory.

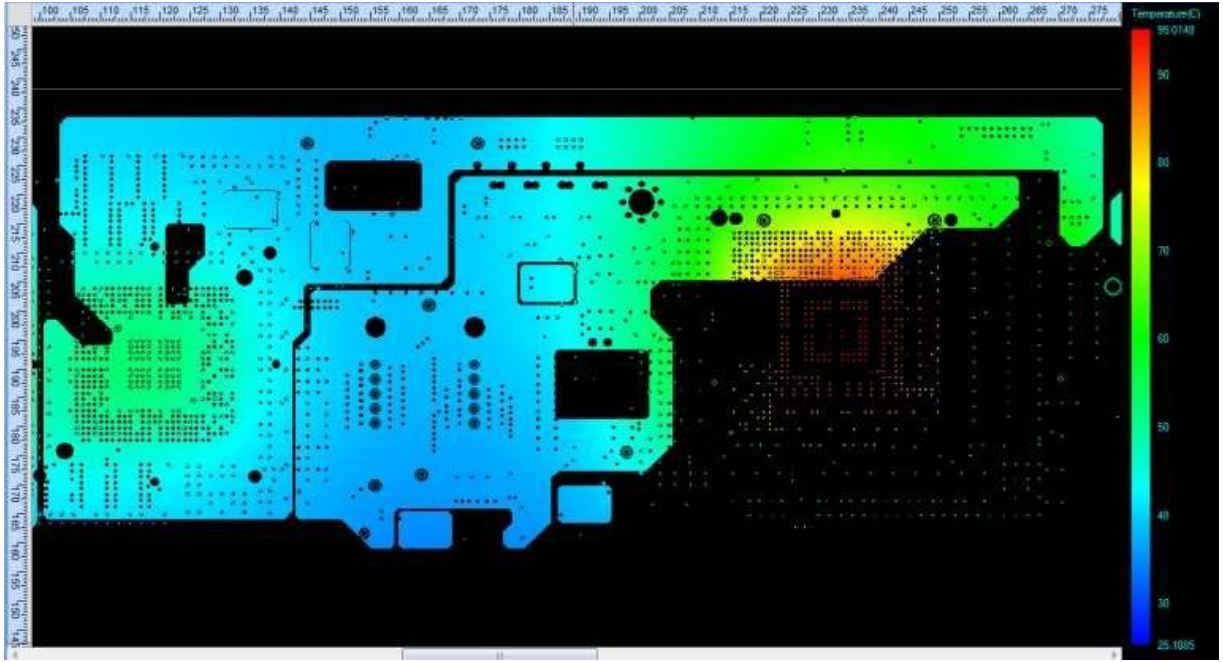
- Using the tool option, the optimum sense line is located. The region highlighted in the below image.

Electrical/Thermal Co-Simulations

- In real time, the joule heating effect caused by the current flow degrades the voltage distribution. So the thermal effect also has to be considered while calculating the IR drop.
- In Sigrity PowerDC, Electrical simulation is combined with thermal distribution analysis and provide results more closer to the real world.
- Also thermal alone analysis can be done in order to know the effect of the joule heating effect.
- Various heat sink model can be studied that best suits the application.

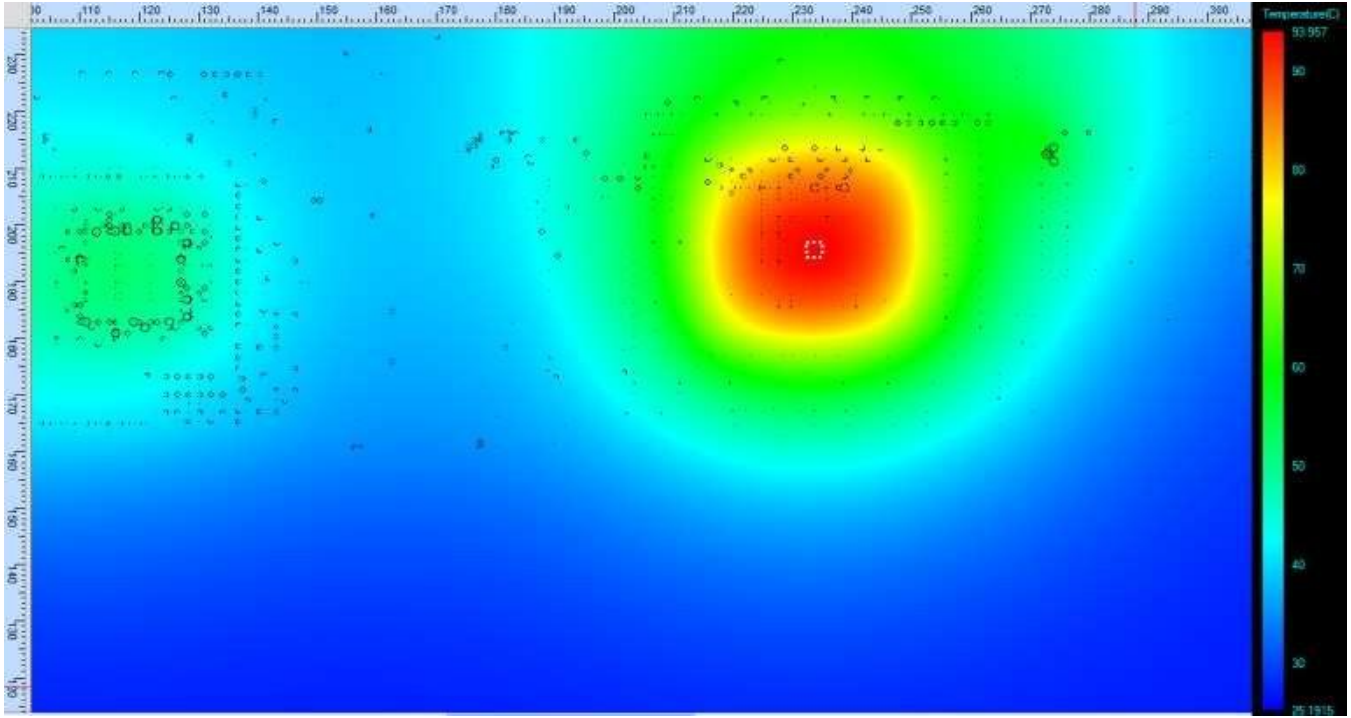
Temperature distribution

PowerDC



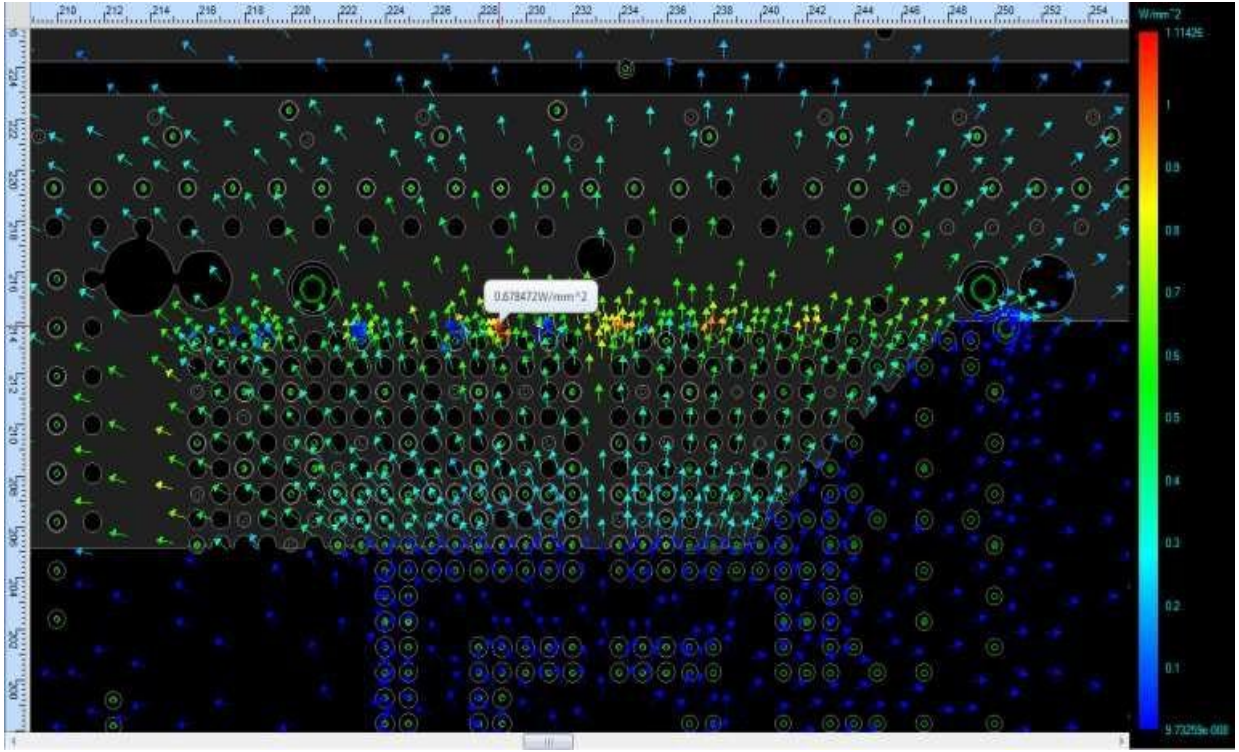
Hot Spot region

PowerDC



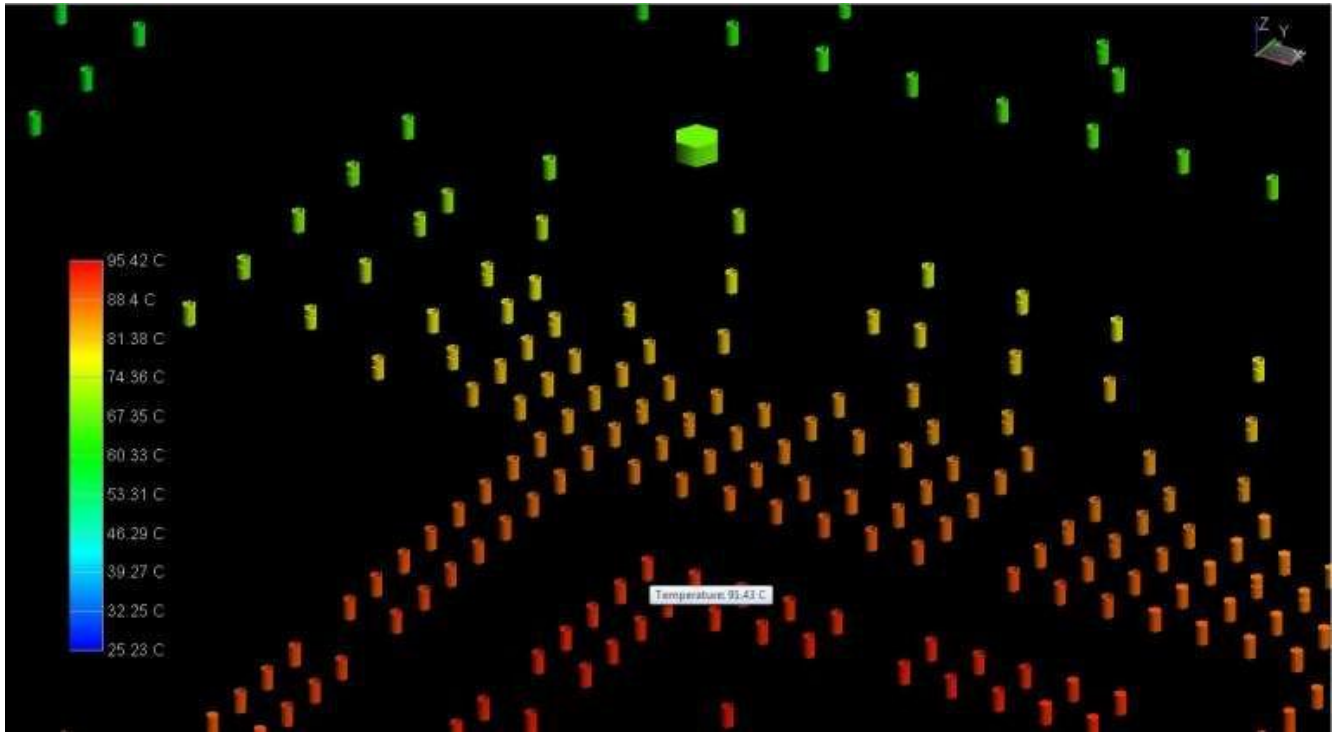
Heat Flux @ Hot spot region

PowerDC



Temperature of via

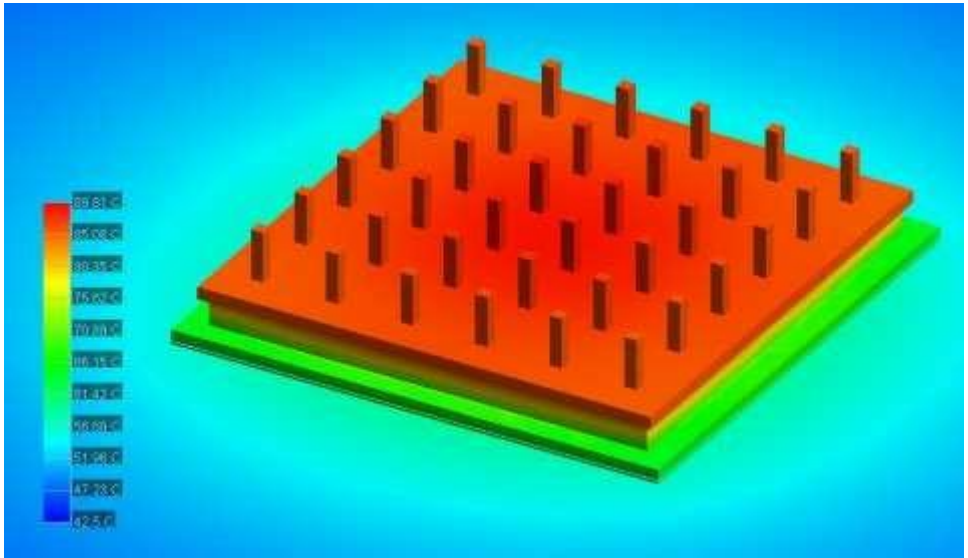
PowerDC



Solution to Thermal issue

PowerDC

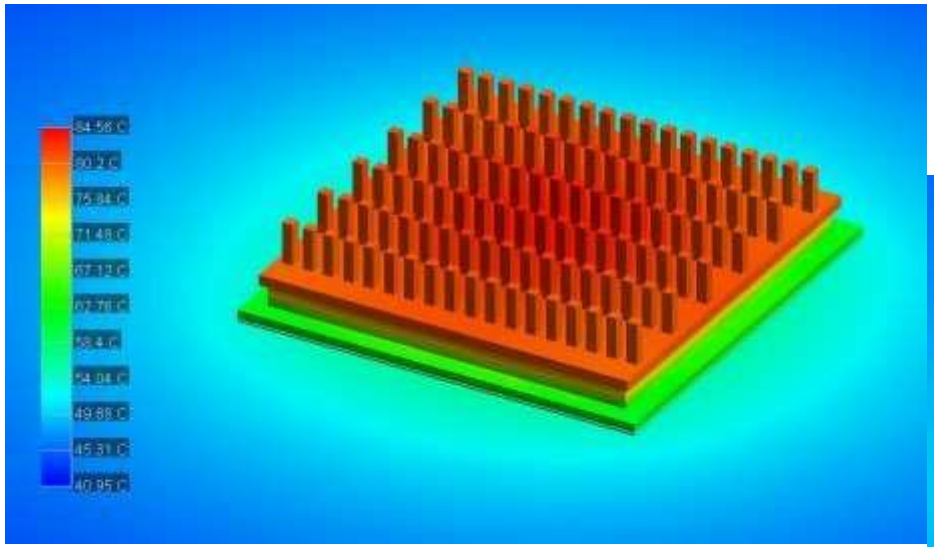
- By analyzing the above results, the damage due to the thermal effect can be quantized.
- Here we found the temperature rise to be more than our threshold and tried to reduce it using heat sink.
- Using simulation tool, various heat sink can be modeled and studied.



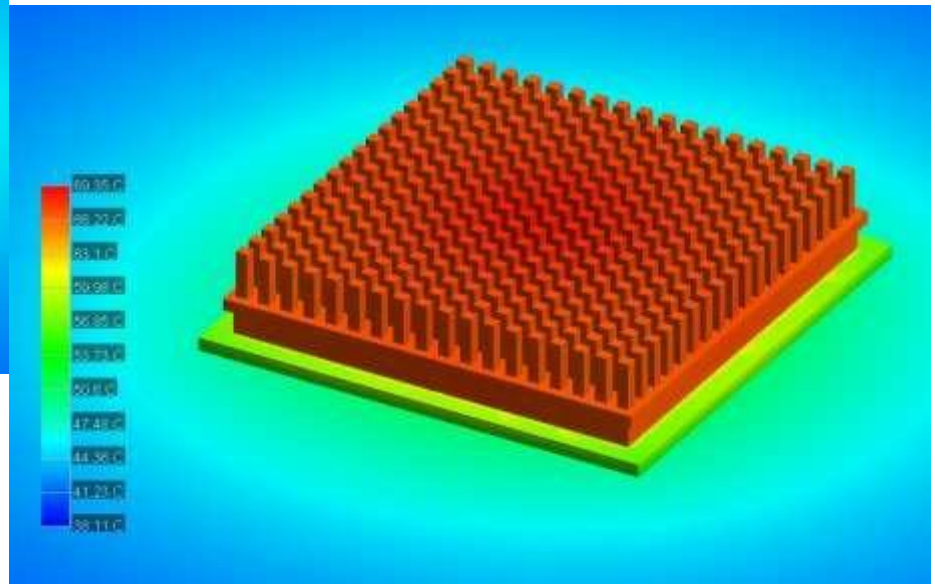
Max temperature = 89.81 C

Effect of Heat sink

PowerDC



Max temperature = 84.56 C



Max temperature = 69.35 C

- With same copper area, but with different orientation of the power plane, the performance of the power planes can be improved.
- Optimal sense pin location is found & used to compensate the voltage drop by 10-30%.
- Electrical/Thermal co-simulation allow us to quantize the joule heating effect and take corrective action.
- The simulation tools provide us with an environment where we can experiment a lot of different cases sans any cost to fab.
- The features of Cadence Sigrity simulation tool like,
  - Sign – Off report
  - Distribution plots 2D & 3D with results overlay option
  - Hierarchical workflow

help us to identify the issues at the design stage itself and reduce the cost & time involved in the re-spin.

- The correlation between the simulation result & real time measurement is also good.

Questions?

Thank you!