Signal & Power Integrity Analysis Services for PCB & Package

Caliber Interconnect Solutions (Pvt) Ltd No 9 B/1, Poombukar Nagar, Thudiyalur, Coimbatore-643034. Tamil Nadu, India.
www.caliberinterconnect.com
Mission & Vision

Mission

“Provide dependable solutions to the satisfaction of the customers through intensive R&D and proven quality control procedures using disciplined workforce.”

Vision

“Developing and applying technological solutions to the benefits of the society that will not affect the safety and living standards of our future generations.”

Quality Policy

“CALIBER INTERCONNECT SOLUTIONS PRIVATE LIMITED is committed to meet and exceed customers expectations through timely delivery of cost effective quality designs through ever improving process and team work.”
CONTENT

• About Caliber
• Business
• Signal Integrity Design
• Summary
Caliber is a fast growing technology services company.

Expertise is High speed PCB, IC package design.

Highly proficient in Signal Integrity, Power Integrity, EMI/EMC analysis.

Specializes in Embedded design services, ATE hardware & Thermal analysis.

200+ highly skilled engineers.

High quality & timely deliverable with attractive cost.

Highest customer satisfaction.
OUR BUSINESS

- SEMICONDUCTOR
- CONSUMER ELECTRONICS
- AEROSPACE & AUTOMOTIVE
- COMMUNICATION & MILITARY

- IC PACKAGE
- HIGH SPEED BOARDS
- SIGNAL INTEGRITY
- EMBEDDED DESIGN
- THERMAL ANALYSIS
ARE YOU FACING THESE ISSUES?

- DATARATES > 1Gbps (clock speed > 500MHz)
- Design your PCB again & again, but still doesn’t work?
- Are you late to the market because of design issues?
- wasting money on several design iterations?
- Design not working across all corners (fast/slow, cold/hot..)
- Design not meeting system timings?
- Poor system margins (eye-height/width)?
- EMI issues after the design in completed??
- Customer is complaining, but you are clueless??

Welcome to
HIGH SPEED DESIGN
SIGNAL INTEGRITY ISSUES
(High speed Design)

- REFLECTIONS
- CROSSTALK
- ATTENUATION
- PROPAGATION DELAY

- GROUND BOUNCE
- POWER SUPPLY NOISE
- EXCESSIVE JITTER
- OVERSHOOT

- ISI JITTER
- SSO JITTER
- RINGING
- UNDERSHOOT

- NON-IDEAL RETURN PATH
- EMI/EMC
• Lumped circuit analysis -> Transmission line analysis
• Full-wave Electromagnetic modeling of all Interconnects (via, connector, microstrip, stripline etc.)
• S-parameter modeling
• Crosstalk & Channel loss analysis
• Power-Distribution-Network (PDN) analysis
  (DC analysis, AC analysis, decoupling estimation)
• Jitter analysis (switching noise, Crosstalk, ISI)
• Eye-diagram plotting
• EMI/EMC analysis

Use state-of-the-art modern simulation tools
SIGNAL INTEGRITY CO-DESIGN

SIGNAL INTEGRITY

POWER INTEGRITY

EMI/EMC

Minimize-cost & Maximize Performance
## SERVICES

**Signal Integrity**
- Pre layout & Post layout
- Serial & parallel interface (DDR 2/3/4, gigabit-SERDES)
- Co-design (IC/package/board)
- IBIS/IBIS-AMI based system SI
- Crosstalk, channel loss, s-parameter, eye-diagram, timing analysis

**Power Integrity**
- DC Analysis (IR drop, voltage/current distribution, density plots)
- AC Analysis (PDN impedance analysis, target impedance optimization, Transient noise estimation)
- Decoupling cap analysis & optimization

**EMI/EMC**
- EMI Radiation
- EMI Susceptibility
- Compliances to various EMI standards during design phase

**Simulation Tools**
- Cadence Sigrity PowerDC, PowerSI, Optimize PI
- Ansys HFSS, Siwave, Designer
- Agilent ADS
High speed serial/parallel interface analysis and design guidelines (DDR2/3/4, multi-gigabit SERDES, USB2.0/3.0, PCIe, XAUI, HDMI, SATA, chip-to-chip IO, FPGA IO)

- Pre-layout & post-layout SI analysis.
- Chip/package/board co-design SSO analysis.
- IBIS/IBIS-AMI based system level SI evaluation.
- Single-ended & Diff-pair design (trace width, spacing and distance to return plane, routing rules)
- Full-wave EM modeling of all kinds of interconnects (via, connector, end-to-end channel)
- Crosstalk and S-parameter modeling of traces and interconnects on package and board.
- EMI/EMC analysis during early design stage.
- The impedance analysis is done using PolarSI.
- Impedance is verified for the given stack up and trace parameters.

**Microstrip Neckdown condition.**

**Microstripline condition.**
S-parameter analysis is done using Ansys tool.

From the S-parameter results, we can get the information about the channel loss and reflection.

Combine channels simulation makes easy comparison between a group of signals.
Via modeling and simulation is done using Ansys HFSS tool.

HFSS is to model 3D structure and to find the best via structure for high speed signals to match the target impedance.
Simulation of high speed SERDES signals gives close eye because of the more channel lengths and package, connectors and vias. SERDES simulation needs IBIS AMI models to do pre-emphasis and equalization for proper eye opening. Proper analysis for ami parameters is very much necessary for High speed SERDES simulation.

The given eye diagram is for 10G XFI channel simulation with and without equalization.
DDR SI ANALYSIS

DATA0_WRITE – 40 ODT

<table>
<thead>
<tr>
<th>ELEMENT</th>
<th>SKEW COMPONENT</th>
<th>SETUP</th>
<th>HOLD</th>
<th>UNITS</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ideal Window (800 Mbps)</td>
<td>Total setup/hold consumed by Transmitter</td>
<td>625</td>
<td>625</td>
<td>ps</td>
<td></td>
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<tr>
<td>Transmitter (IMX6SDLAE)</td>
<td>tdH/tdS</td>
<td>205</td>
<td>280</td>
<td>ps</td>
<td>From data sheet</td>
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<tr>
<td>DRAM device</td>
<td>based on slew rate (simulation)</td>
<td>125</td>
<td>150</td>
<td>ps</td>
<td>from SDRAM datasheet</td>
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<tr>
<td>DRAM derating</td>
<td></td>
<td>50</td>
<td>88</td>
<td>ps</td>
<td>calculated from SDRAM datasheet</td>
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<tr>
<td>Controller + SDRAM jitter</td>
<td>Available setup/hold time</td>
<td>380</td>
<td>518</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>Total Interconnect</td>
<td>DQ/DQS eyediagram setup/hold margin (Crosstalk + ISI)</td>
<td>519.2</td>
<td>607.3</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td></td>
<td>DQ-DQS skew</td>
<td>10.8</td>
<td>17.7</td>
<td>ps</td>
<td>From Simulation</td>
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<tr>
<td>Total Budget Consumed by Controller, DRAM and Interconnect</td>
<td>Transmitter + DRAM + Interconnect</td>
<td>495.8</td>
<td>545.7</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>Margin</td>
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<td>129.2</td>
<td>79.3</td>
<td>ps</td>
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</table>

Analysis for different ODT condition and checking the best set up and hold time margin calculation for Read/Write is necessary in DDR simulation.
➤ Pre- & post-layout PI simulations.

➤ AC & DC analysis of package & board.

➤ Analyze and verify power supply quality at chip, package & board level.

➤ Ensure required and effective power distribution and power supply decoupling.

➤ Target impedance estimation and optimization.

➤ Z11 estimation and optimization to meet target impedance.

➤ Decoupling cap estimation and optimization.

➤ Power-ground loop inductance & stack-up optimization.

➤ Package/board power & ground parasitic extraction (R,L,C)

➤ IR drop analysis and give recommendation about placement of components.

➤ Comprehensive report generation and documentation for better customer support.
PI- IR DROP SIMULATION

IR drop Simulation

![IR drop RESULT](image)

- **Voltage distribution in Ground Plane—showing groundbounce**
- **Voltage distribution in signal Layer – drop at pin and Via**
High loop inductance - poor cap placement
• Power Plane Impedance Analysis

Power impedance optimization graphs with different decap schemes
EMI/EMC Checking according to **CISPR Class A Standard**

**GENERAL INFORMATION**

- Board: BOARD_2.hyp
- Total number of nets: 775
- Total number of components: 75
- Board temperature: 20.0 degrees C
- Default IC model (used for quick analysis if IC model is missing)

- IC driver rise/fall time: 2.000 ns
- IC driver switching voltage range: 3.00 V
- IC driver output impedance: 1.0 ohms
- IC input capacitance: 7.0 pF

**NET INFORMATION**

- NET = CH23
  - EMC SIMULATION RESULTS
  - Net's EMC is within selected limits

- NET = CH42
  - EMC SIMULATION RESULTS
  - Net's EMC is within selected limits

- NET = CH39
  - EMC SIMULATION RESULTS
  - Net's EMC is within selected limits

- NET = CH124
  - EMC SIMULATION RESULTS
  - Net's EMC is within selected limits

- NET = CH141
  - EMC SIMULATION RESULTS
  - Net's EMC is within selected limits

**EMC STANDARD CHECKING REPORT BASED ON CISPR**
Why Caliber Interconnect Solutions?

• Expert Technology Service provide
  – Expert level experience reduces time to market
• Right Processes
  – Right Simulation tools
  – Proven Quality Control procedures and practices
• Customer Focus
  – Commitment to results
• Competitive cost structure
  – Fixed cost & hourly contract model
• Leadership Team
  – Technology focused
  – Long history of successful Entrepreneurship
BUSINESS MODELS

- Build, Operate, Transfer
- Fixed Model
- Time and Material Basis
- Off Site Development Centre
- On Site Resources

Caliber Interconnect Solutions Pvt Ltd
Global Presence

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