



GROUND BOUNCE CAUSE, EFFECT AND SOLUTION

Advancement in technology leads to miniaturization of electronic devices. The increase in functionalities is inversely proportional to the geometries of the electronic system. The factors which drastically changed in electronic devices in recent days are size, no. of pins and edge rates. Number of pins increased to cater the increase in I/O counts and edge rates have reduced considerably to meet better timing margin. This miniaturization results into adverse effect which tends to decrease the performance of system. One such effect is Ground Bounce/Simultaneous Switching noise.

CAUSE

In digital system the exchange of data takes place in the form of 1's and 0's. The output driver generates these binary symbols through load capacitor. Basically, a capacitor charges and discharges to implement transition from 0 to 1 and 1 to 0 respectively. At higher edge rate, connecting leads exhibit inductance. In Fig.1 L is the lead inductance present in input and ground path interconnect when transition is from 0 to 1 and 1 to 0 respectively. When more no. of I/O switches the current rush through these interconnects. The variation in current across interconnect (Inductor) causes voltage drop. This voltage drop is represented as:

$$V = L \frac{di}{dt}$$

There are two scenarios in which this adverse effect takes place :

1. Transition from 0 to 1

In this case the load capacitor charges and the flow of current is toward output.

2. Transition from 1 to 0

In this case the load capacitor discharges and the flow of current is toward sink.

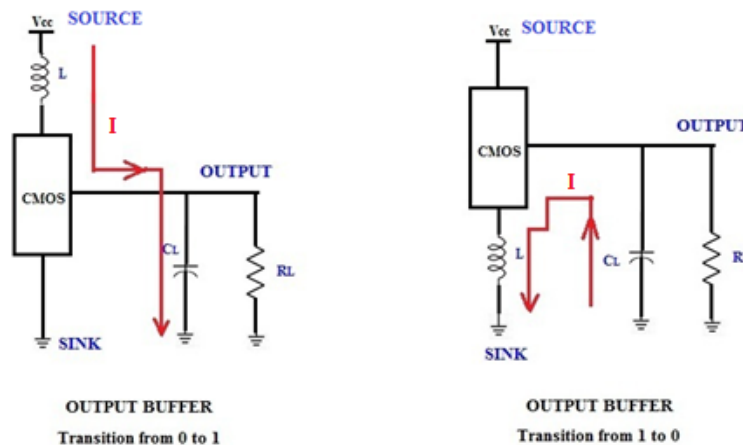


Fig.1

In both scenarios noise is induced in the system. The noise due to scenario 1 is known as **VCC-Sag** and because of scenario 2 is called as **Ground Bounce**. The effect of VCC-Sag is small compared to Ground Bounce.



EFFECT

For 1 to 0 transition the current flows toward system ground to discharge the capacitor. This current flows from device ground (die) to system ground through Wire Bond (connecting die and package), package traces and solder ball to board ground. In case of fast switching of I/O pins these interconnecting elements acts as inductor. (Fig.2). Due to the variation in current across inductor voltage drop occurs. Now, the Device ground (Die GND) is not same as System ground (Board GND) as in ideal case.

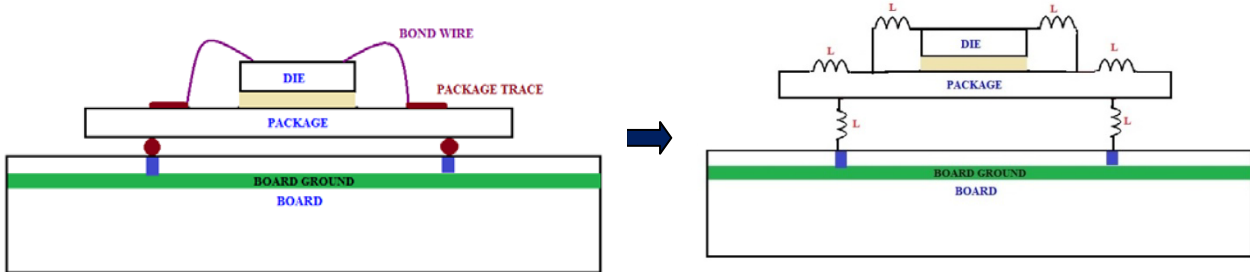


Fig.2

In ideal case, Device ground and system ground are equal so output signal have same voltage value. But due to ground bounce the device ground have some voltage drop because of which output voltage level varies from original values. This is shown as below.

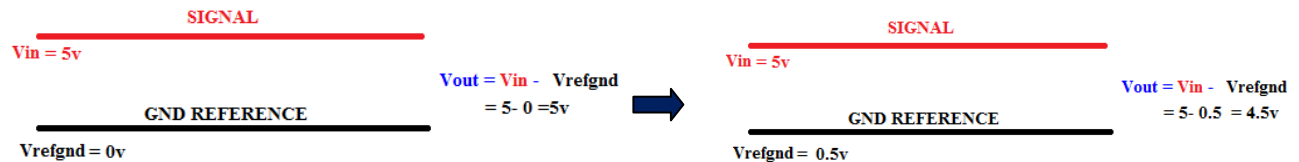
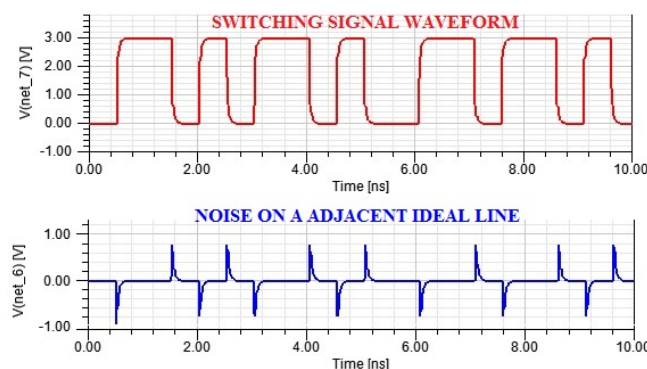


Fig.3

Ground bounce also acts as crosstalk on the ideal line next to the switching line. Because of voltage drop across inductance in return path noise gets induced in the ideal line.



Ground Bounce is dominant when more no. of outputs switches simultaneously. This is reason why it is also called as **Simultaneous Switching Noise (SSN)**.



SOLUTION

The main reason of ground bounce is inductance in return path, simultaneous switching of adjacent I/Os fast edge rates etc. If these factors are taken care then the effect of ground bounce can be minimized. Some of the major sources for the ground bounce are:

- Inductance in return path
- Sharing the common return path
- Edge rate
- Connectors and Vias

- 1) Inductance in return path cannot be eradicated fully but it can be minimized. Instead of wire bond technology if flip chip technology is used inductance due to bond wire can be eradicated. By implementing this the Ground Bounce is improved by 72%.

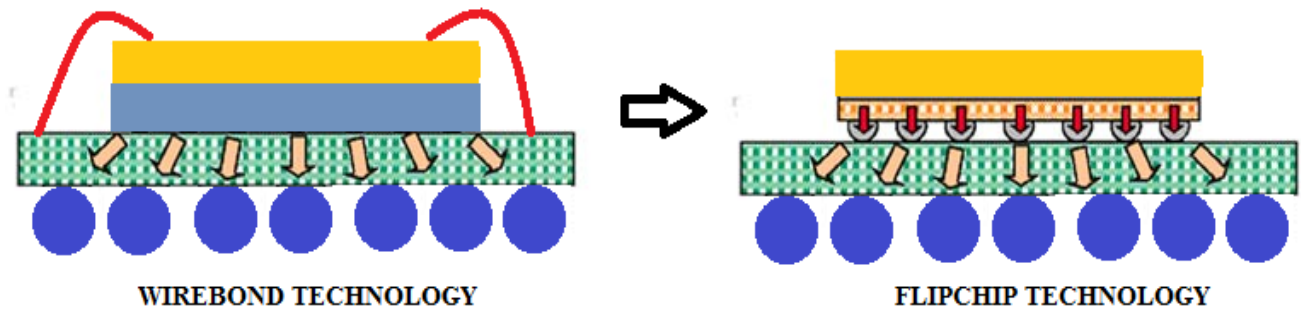


Fig.4

- 2) When the return current of the signals shares the same return path it will induce the ground bounce in the network. It is advisable to have different return path for analog and digital signals to overcome this effect. Here $I_1 = I_2$ but the Inductance L_{21} and L_{22} are different. Because of this GND bounce is induced in top layer.

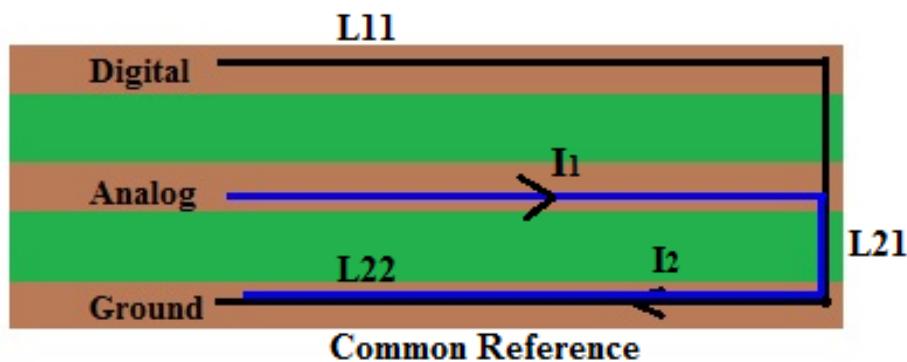


Fig.5

- 3) Edge rate ($\Delta V/\Delta T$) of the signal will cause the major impact on the ground bounce. Higher edge rate increase the ground bounce whereas lower edge rate will decrease the ground bounce.

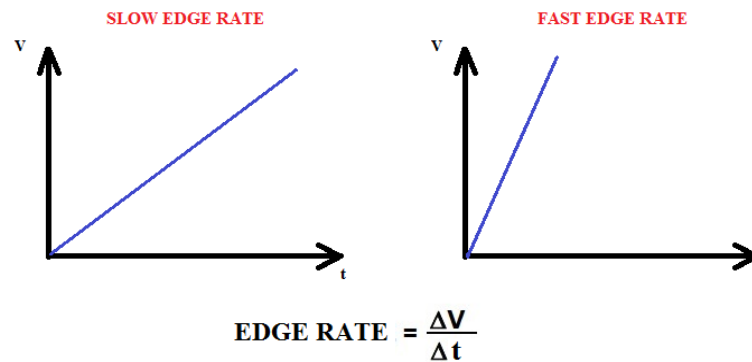


Fig.6

- 4) The noise immunity can be increased by using programmable Vcc and GND pins. These programmable pins are basically I/O pins. All the unused pins are programmed to drive ground.



By having the highlighted I/O pin connected to GND the ground bounce can be improved by 42%.

- 5) Using Series resistor. Series termination resistor reduces the variation of current by reducing the rate of change of output on the network. By using series termination resistor the edge rate reduces. Rs value is usually around 10 Ω to 33 Ω.

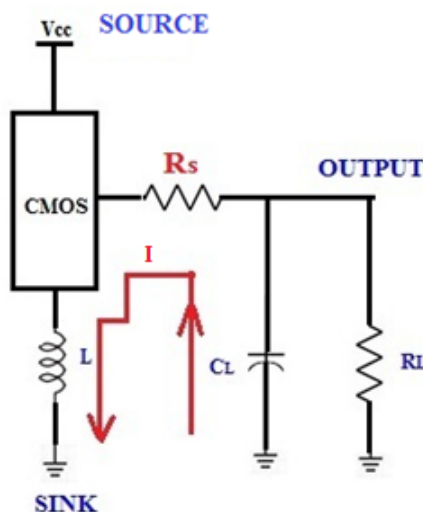


Fig.7