



SIGNIFICANCE OF PLACEMENT HIERARCHY FOR DE-CAPS; BULKCAPS

The primary rule followed for the placement of the De-Cap & Bulk cap is *“The De-Caps with lower capacitance should be placed very close to the Die/ IC, followed by the next higher value De-caps and then the Bulk caps”*. The designer can follow the rules and finish the placement with ease. But not many think of the reason for such a hierarchical placement rule. Does this rule have any electrical significance or not? This article tries to explain the reason beyond such a rule, first technically and then using an analogy.

Purpose of De-Caps and Bulk Caps

Voltage level for an IC is fixed. But during the operation of the IC, power demand fluctuates due to which the current consumption of the IC varies. Also the voltage level at the IC is decreased. It is this current fluctuation that creates all the issue. At this juncture try to recall the 2 elementary formulae studied in your basic circuits classes.

#1 Voltage across the inductor is given by,

$$v = \frac{d}{dt} (L I) = L \frac{dI}{dt}$$

#2 Current through the capacitor is given by,

$$I = \frac{d}{dt} (C V) = C \frac{dV}{dt}$$

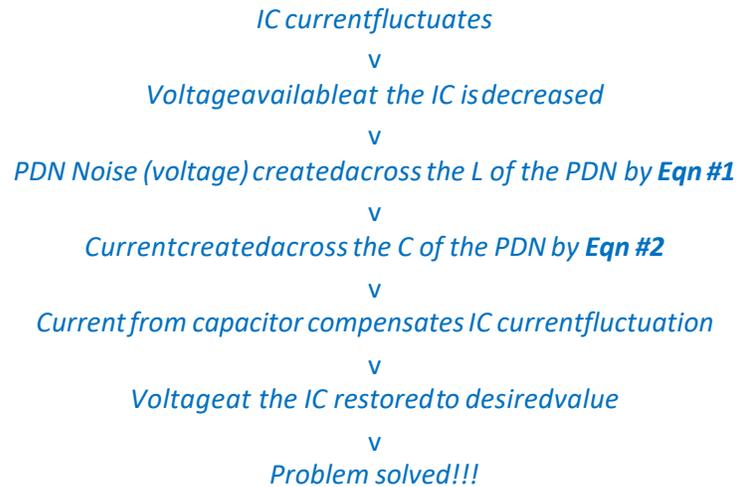
By equation #1, as the current consumption of the IC varies, a voltage is created across the Inductor of the PDN (Power Delivery Network. Every PDN has in-built RLC). The voltage created across the PDN is directly proportional to the inductance of the PDN and the amount of current fluctuation. This voltage is the PDN noise, when the IC current consumption is varied. How to reduce this noise?

One way is to reduce the L of PDN, as evident from equation #1. Another way is to reduce the current fluctuation by supplying extra current and bringing the current to a constant level quickly. These changes should occur in very small time intervals (ns range). But the Voltage Regulator (VRM), that acts as main source cannot react quickly to compensate this sudden change in the current variation. What is the solution, who will supply the extra current? Hope you guessed it right.

Equation #2 provides the solution. As the voltage varies, current across the capacitor increases (equation #2). Thus the capacitor of the PDN provide instantaneous current jolt which helps to maintain constant voltage across the IC. Here capacitor acts as a current source. The current is directly proportional to the C of the PDN.



The whole chain reaction can be consolidated as below,



The simple mantra to reduce the PDN noise is; to reduce inductance of PDN and increase capacitance of PDN as much as possible. This is the reason, it is sometimes mentioned that Inductance is an Enemy and capacitance is a Friend of a Layout designer. In short De-Caps and Bulk caps are added in the layout for this very reason.

PLACEMENT HIERARCHY

Now coming to the placement hierarchy, as per the above discussion, the time in which the current fluctuation is made constant, is very critical. This time if long, can have adverse effect on the performance of the IC. The reaction time of the Capacitors (Transient time for the capacitor to charge/discharge) is their inherent property given by the term Time Constant = RC (R- Parasitic resistance of Cap, C- Capacitance value). Lower the value of the capacitor, faster it can react (charge/ discharge) and vice versa.

Thus de-caps with the lowest capacitance value is the first line of defense against the PDN noise caused due to the current fluctuation. As they are of low value, they can react faster. This is the reason, the de-caps are placed as close to the IC. But these can supply only a small amount of current for brief time (nsec). Their job has to be taken over by another current source that can supply higher current for more time. Bulk caps (higher caps value than the de-caps), step in and do their share to bring back the current to constant value. The Bulk caps can supply current for msec range and are placed next to the de-caps.

VRM - The Big Brother by now is ready to take the whole situation under its control. Thus it is kind of a team work that helps to contain the PDN noise. The plane capacitance of the power net is also a part of this team. The caps though have various characteristics, each play a very critical role. This team can perform when the comrades are placed in their respective position in the battle. Change the position of a frontline soldier to rear, and you are sure to lose the battle. The same applies to the position of the capacitors.



It is always,

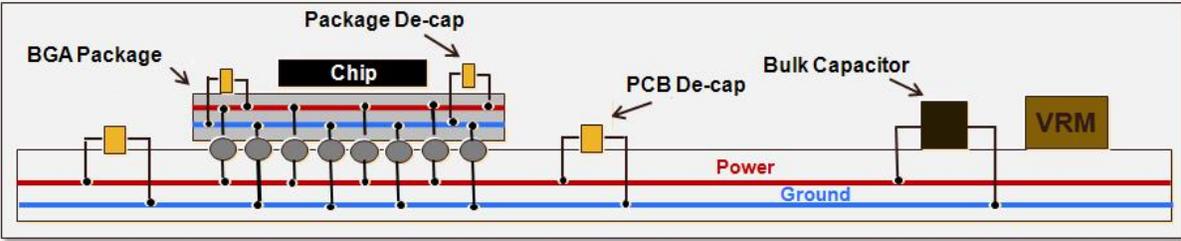
IC >> Lower value De-Caps >> Higher value De-Caps >> Bulk Caps >> VRM

The caps value, reaction / transient response time decide the position of each of these soldiers.

ANALOGY

A simple analogy to this content is the position and role of the power backups that we use for domestic usage. Consider there is a power failure for some reason. To keep the critical appliances running, the UPS or Power Cabinets (analogy to De-Caps) act as the first line of defense. They can react fast, but can supply low power for brief time. Then the Gensets (analogy to Bulk caps), which can provide large power for say up to 12hours is used for the purpose. The power station (analogy to VRM) by now is back to form and can supply power for days.

POWER CABINETS	GENSET	POWER STATION
		
Emergency source	Intermediate source	Main source
Lower power capability	Medium power capability	Larger power capability
Quickest to react / respond	Slower to react / respond	Slowest to react / respond
Supply for brief time	Supply for considerable time	Supply for longer time

DE CAPS	BULK CAPS	VOLTAGE REGULATOR
		
Emergency source	Intermediate source	Main source
Lower capacitance value	Higher capacitance value	-
Quickest to react to current fluctuation in IC	Slower to react to current fluctuation in IC	Slowest to react to current fluctuation in IC
Supply for brief time	Supply for considerable time	Supply for longer time

Note: The resonance of the capacitors also decides on the placement of the capacitors, but this factor is not considered for this article.