

Caliber Interconnect Solutions

Design for perfection



FPGA DESIGN SERVICES

(ISO 9001:2008 CERTIFIED)

Caliber Interconnect Solutions (Pvt) Ltd No 6,1st Street Gandhi Nagar, Kavundampalayam, Coimbatore-30. Tamil Nadu, India. www.caliberinterconnects.com



Mission & Vision

Mission

"Provide dependable solutions to the satisfaction of the customers through intensive R&D and proven quality control procedures using disciplined workforce."

Vision

Developing and applying technological solutions to the benefits of the society that will not affect the safety and living standards of our future generations."

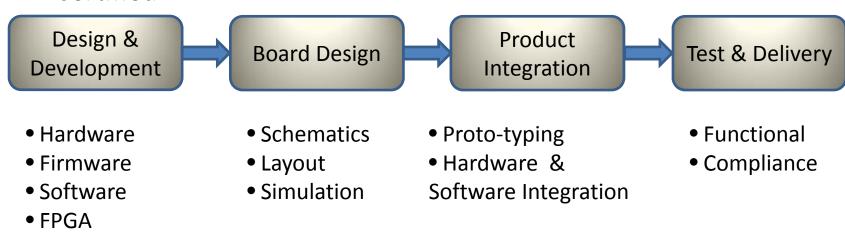
Quality Policy

CALIBER INTERCONNECT SOLUTIONS PRIVATE LIMITED is committed to exceed customers expectations through timely delivery of cost effective quality designs through ever improving process and team work.



Profile

- Providing Integrated Product Engineering Services to Global Semiconductor and Technology Companies
- Expertise Under One-Roof
 - Concept Development to Product Delivery
- Unique combination of expertise in Hardware, Firmware/Software, FPGA, Board Design and Product Integration
- Proven Quality Control Procedures and Practices ISO 9001 Certified





About us

Fast growing Electronics & Embedded design services company. 200+ specialized and High Caliber Engineers Specializes in Embedded System Design Services Specializes in Hardware Design IC Packaging Solutions. Design and Fab of HDI's High Quality & Timely delivery for attractive cost. Highest customer satisfaction. Over 15 Years in the industry.



Industry associations



Member of Indo American Chamber of Commerce



Member of National Association of Software and Services Companies



Member of Indian Electronics and Semiconductor Association



Member of Dun & Bradstreet Services



ISO 9001:2008 Certified by BUREAU VERITAS



FPGA Design Services

- VHDL and Verilog Firmware
- Hardware
- Design and Development
- Test Bench Development and Verification
- RTL Coding



FPGA Design Services

- Peripheral/Bus Interface Logic development
 - PCI-Express, LVDS, PPI, USB
 - Memory DDR4, DDR3, DDR2
 - NAND Flash, SD/MMC
 - I2C, SPI, UART, Proprietary
- Algorithm/IP Core development
 - CODECs HDMI, MPEG
 - Image Processing
 - Encryption/Decryption
 - LUT, DDS, Dual Port RAM, Filters
 - Custom IP Cores
- 3rd Party Module Integration
- Soft Core Processors/IPs
- FPGA IP Validation & Optimization



Tools and Devices

- IDEs Xilinx ISE, ispLever/Lattice Diamond, Actel Libero, Altera Quartus II, Atmel WinCupl
- Simulators Simulink, ModelSim, Cadence, ISim, Aldec Active-HDL, Synopsis VCS
- Devices
 - Xilinx Virtex UltraScale, Spartan, XC9500XL
 - Altera Stratix, Cyclone
 - MicroSemi proASIC, IGLOO
 - Lattice ispMach

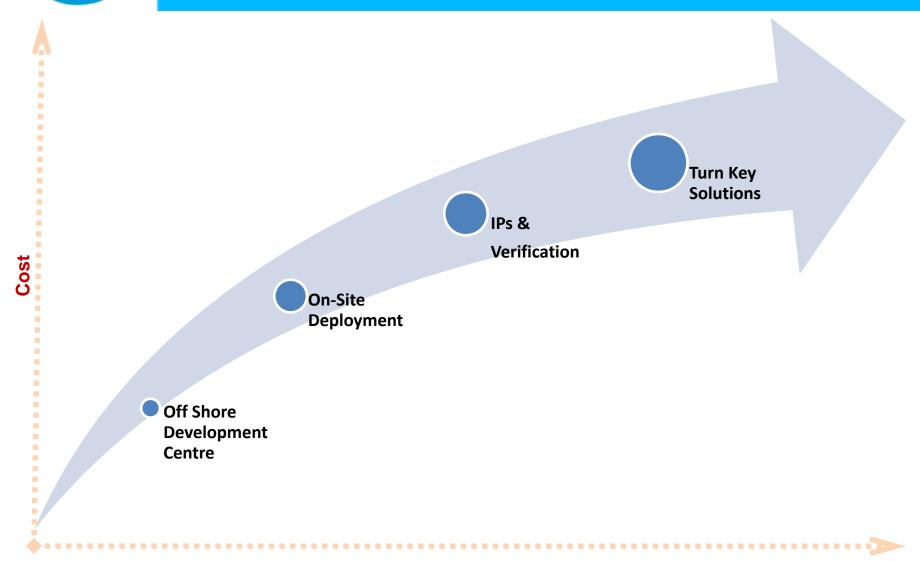


Why Us?

- Expertise
 - Design Perfection
 - Reduced time to market
- Processes
 - Proven Quality Control procedures and Practices
- Customer Focus
 - Commitment to results
- Team
 - Technology focused
 - Versatile



Business models





FEW CASE STUDIES



USB UVM Verification

Project: Test Bench for USB 3.0 IP verification

Mode: Offsite Development

Team Size: 4

Duration: 1 Month

Description:

Functions of Test-Bench:

- 1. Generate stimulus
- 2. Apply stimulus to the DUT
- 3. Capture the response
- 4. Check for correctness

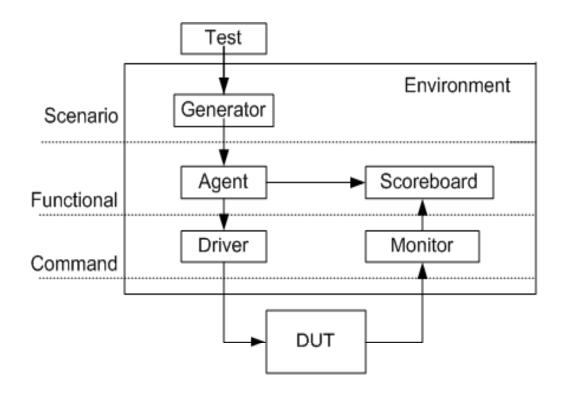
Algorithm: Universal verification methodology (UVM)

Environment: System Verilog, Synopsys VCS



USB UVM Verification

[Continued...]



Test-Bench Layers



Home Automation Server

Project: Server for Home Automation modules

Mode: In-house Development

Team Size: 4

Duration: 6 Months

Description:

The server board acts as gateway and links external clients with modules inside the building.

A soft-core MicroBlaze Architecture was implemented on Xilinx Virtex-6 FPGA with the following interfaces: DDR3, NOR Flash, HDMI, 1000BASE-T (GigE), 10BASE-T, SPI, I2C, IrDA, UART & Audio CODEC. Developed / Customized IPs and did verification of all the functional modules / IPs with test-bench programs.

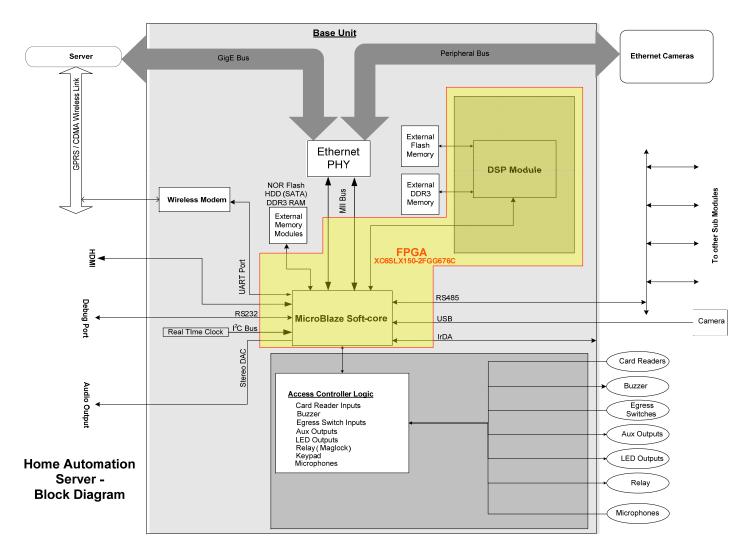
Tools Used: Xilinx ISE Design Suite, ModelSim

Device Used: Xilinx FPGA Virtex-6



Home Automation Server

[Continued...]





Probe Data Interface for Aircrafts

Project: Probe Data Interface for the Landing

Gear Control System

Mode: Offsite Development

Team Size: 4

Duration: 3 Months

Description:

The Probe Data Interface (PDI) is a high speed data acquisition system combined with waveform synthesizer, which is used for measurement of various environmental parameters.

This data is used by the controller to decide on deployment of landing gears during landing of the aircraft.

Algorithm used: DDS, LUT, FIR Filters

Interfaces developed: LVDS, ADC/DAC interfaces, Host Controller interface

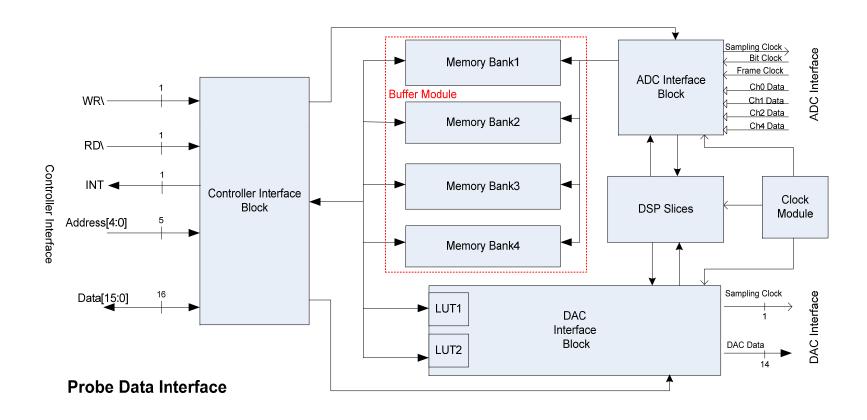
Tools Used: Xilinx ISE Design Suite, ModelSim

Device Used: Xilinx FPGA Virtex-6



Probe Data Interface for Aircrafts

[Continued...]





Industrial camera interface module

Project: Image Processing Module

Mode: Offsite Development

Team Size: 4

Duration: 3 Months

Description:

The image processing module consists of PPI interface to a host controller, DSP Slices and CameraLink LVDS interface to array of cameras and UART for configuring the cameras.

Algorithm used: Image Processing, Image Recognition

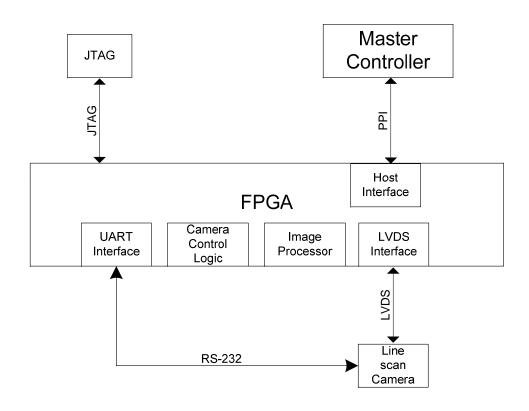
Interfaces developed: UART, LVDS, PPI

Tools Used: Xilinx ISE Design Suite, ModelSim

Device Used: Xilinx FPGA Virtex-3



Industrial camera interface module [Continued...]





ATE Probe card

Project: Probe card

Mode: Offsite Development

Team Size: 2

Duration: 1 Month

Description:

Probe card contains Tester interface, Command decoder, Look-up-table (LUT), Encoder for an array (256) of ASW (Analog switches).

There are four types of commands from the tester that manipulate these ASWs.

Algorithm used: Proprietary CODEC

Interfaces developed: Tester Interface, ASW Interface

Tools Used: Xilinx ISE, ModelSim

Device Used: Xilinx Virtex-6



Automated tester for iPod

Project: Automated Tester unit for iPod

Mode: Offsite Development

Team Size: 5

Duration: 3 Months

Description:

The module acts as an interface for a host computer, a proprietary communication module and an iPod to run a set of BIST commands and generates test results for the host computer

Algorithm used: Clock Jitter Analysis

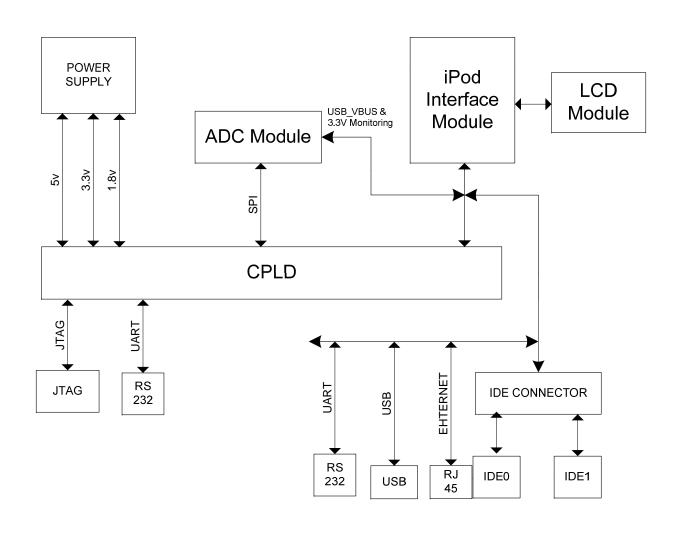
Interfaces Developed: UART, ADC, LCD Panel

Tools Used: Xilinx ISE Design Suite

Device Used: Xilinx CPLD XC2C512



Automated Tester for iPod [Continued...]





H-Bridge Protection in IGBT based Inverters of 10kW and above capacities

Project: H-Bridge Protection Logic for Inverters

Mode: In-house Development

Duration: 2 Months

Description:

The protection scheme was implemented using Lattice ispMACH4000 CPLD. The logic receives VPWM waveforms from a DSP controller, decodes them and drives individual IGBTs. It monitors error conditions in input waveforms, output switching waveforms and internal processing. Upon error condition, it shuts down all the IGBT switches within nano-second delay and protects them from catastrophic consequences.

Verification was done extensively with suitable teat-bench programs.

Tools Used: ispLever, ModelSim

Device Used: ispMACH4000 CPLD



Our Locations

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Thank You!!

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